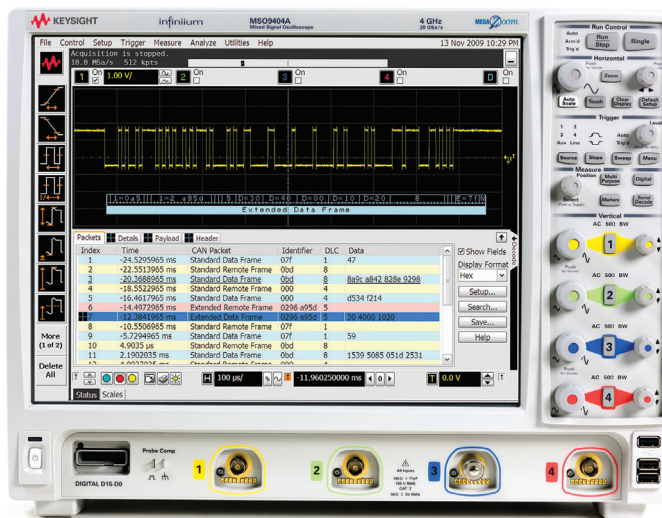


# Keysight Technologies

## 81100 Family of Pulse/Pattern Generators

Simulation of Jittering Synchronization  
Signals for Video Interfaces

Technical Overview  
Version 2.0





## Introduction

This product note describes how R&D engineers in the communication industry use Keysight Technologies, Inc. pulse generators for the development of video interfaces for projection units.

Several data communication companies develop interfaces between Local Clock Oscillators (LCOs) and video, TV, or computers for overhead projection units. It is very important for them to stay up-to-date with the rapidly changing video interfaces in computers, and to have test equipment that can simulate these different interfaces (such as HDTV interfaces). These interfaces vary from 33 MHz to 80 MHz.

A critical indicator of the quality of their design is its sensitivity to a jittering distributed clock signal, both in frequency and amplitude.

## Required equipment for Lab 2

- 1 x pulse/pattern generator (81150A or 81160A)
- 1 x Infiniium oscilloscope
- 4 x BNC cables

## How to hook up the instruments

- Connect strobe out 2 (pulse/pattern generator) to channel 3 (scope).
- Connect output 1 (pulse/pattern generator) to channel 1 (scope).
- Connect output 2 (pulse/pattern generator) to channel 2 (scope).
- Connect trigger out 2 (pulse/pattern generator) to channel 4 (scope).

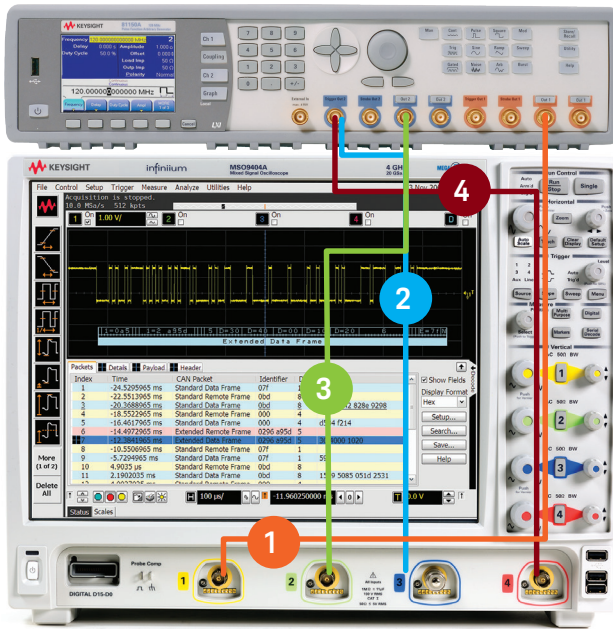


Figure 1. The setup of a Keysight pulse generator and Infiniium oscilloscope

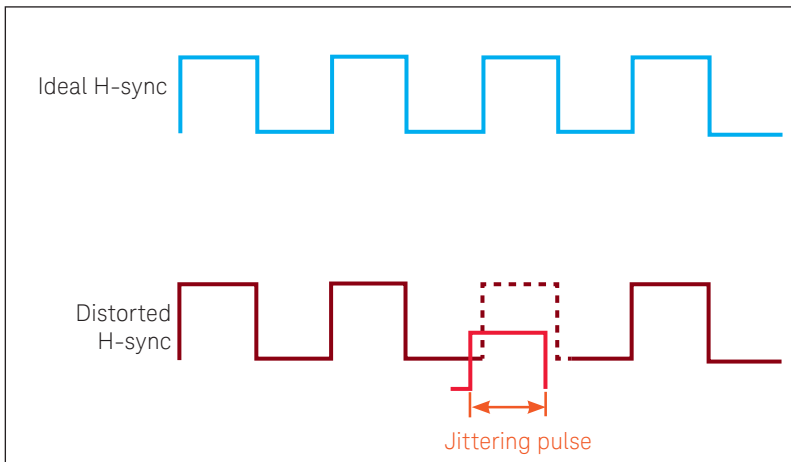


Figure 2. Jittering distributed clock signal

To simulate jittering synchronization signals with a pulse generator, we need:

- Two output channels with channel addition

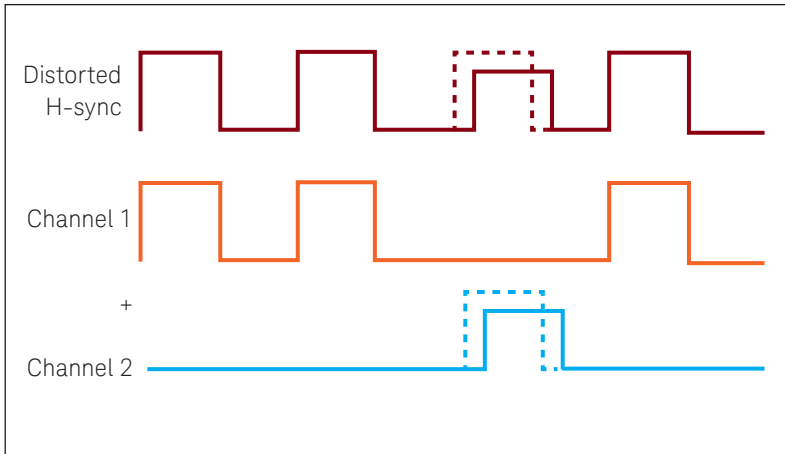


Figure 3.

- Programmable bit patterns up to 90 MHz frequency

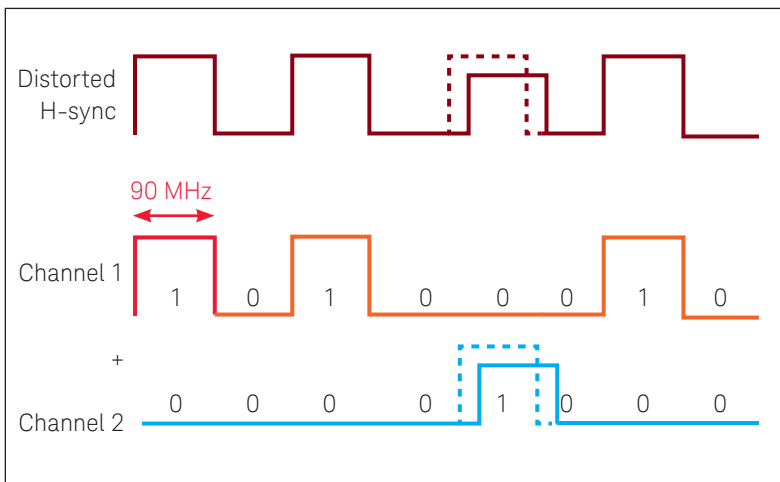


Figure 4.

- Variable delay and variable level

Follow the steps on the next pages to set up the correct parameter values on the front panel. Then review the pulses on the oscilloscope.

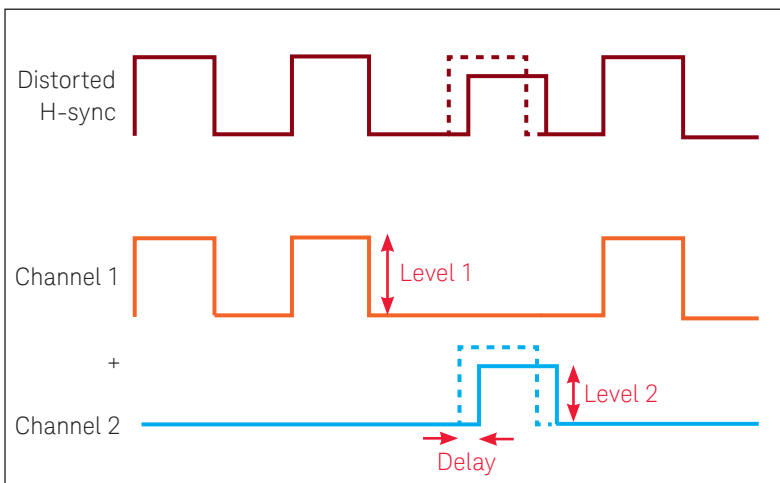


Figure 5.

**STEP 1.** First, reset the instrument by pushing Store/Recall and selecting 'Set to default'.

**STEP 2.** Enable 'Continuous trigger mode' (select 'cont') and select 'Pulse Waveform' ('Pulse') for channel 1 and channel 2.

**STEP 3.** Set channel 1, as shown in Figure 6.

Frequency: 90 MHz  
 Duty cycle: 50%  
 LeadE: 5 ns  
 High: 1 V  
 Low: 0 V

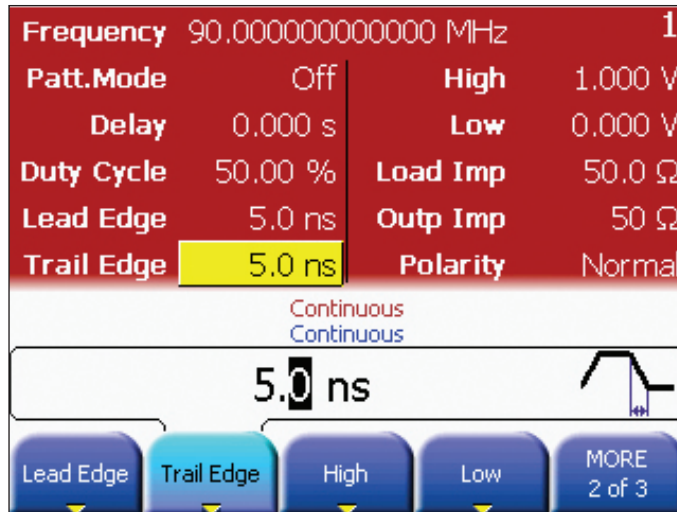


Figure 6. Step 3.

**STEP 4.** Set channel 2, as shown in Figure 7.

Frequency: 90 MHz  
 Duty cycle: 50%  
 LeadE: 5 ns  
 High: 950 mV  
 Low: 0 V

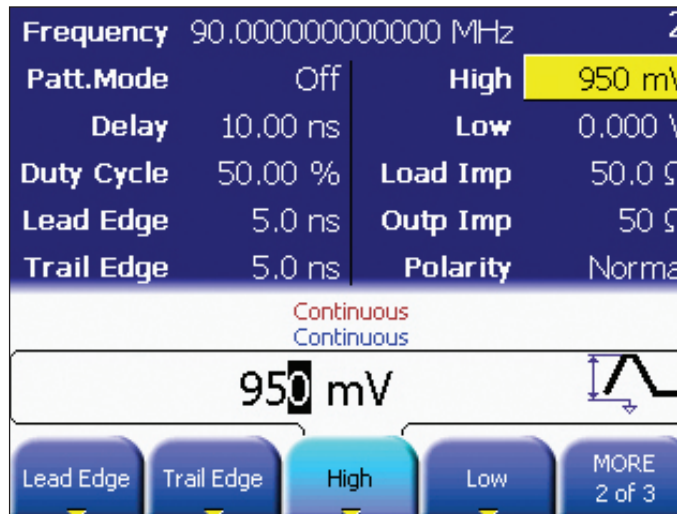


Figure 7. Step 4.

**STEP 5.** Choose channel 1; select 'pattern mode,' and push 'Edit Pattern' to create a new channel.

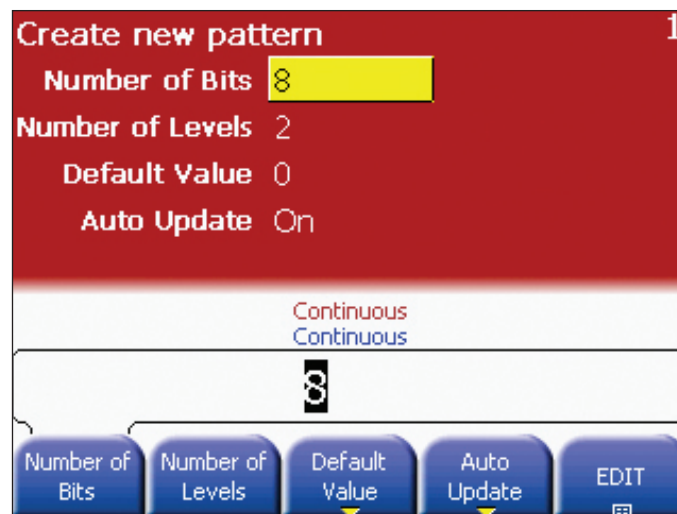


Figure 8. Step 5.

**STEP 6.** The number of bits are 8. Set the bits by starting with the last bit.

Note: Pattern is 10100010.

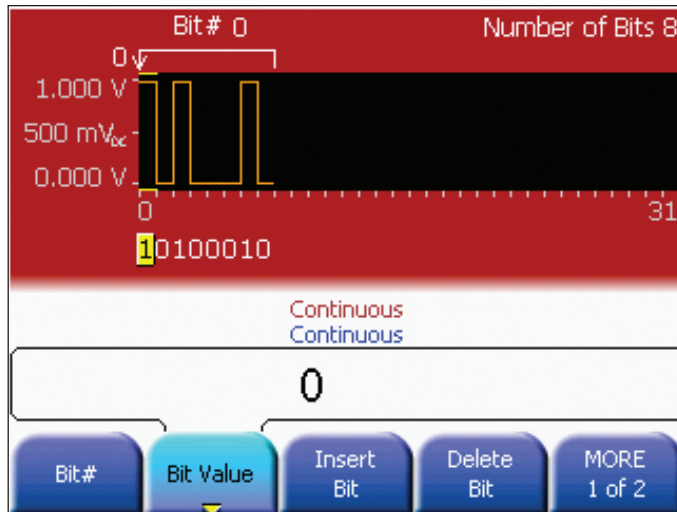


Figure 9. Step 6.

**STEP 7.** Perform steps 5 and 6 for channel 2.

Note: Pattern is 00001000.

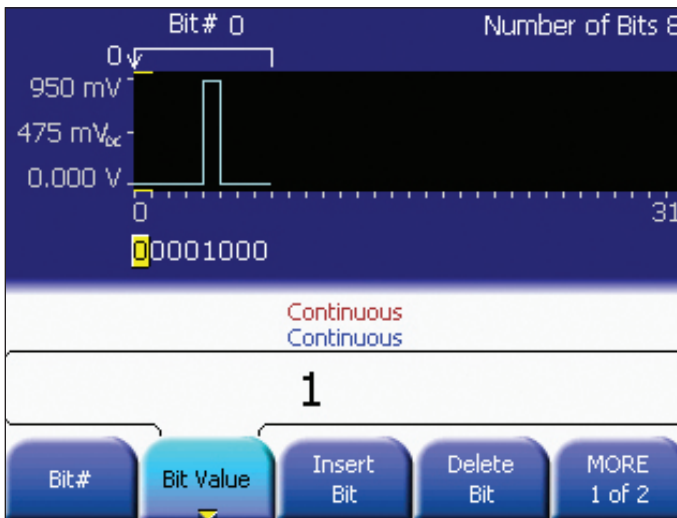


Figure 10. Step 7.

**STEP 8.** Review the signals on channels 1 and 2.

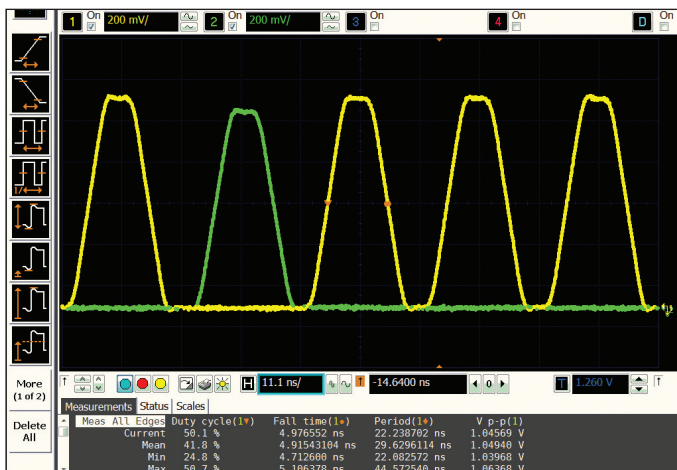


Figure 11. Step 8.

**STEP 9.** Press 'Coupling,' so that both pulses begin at the same time. Add channels by choosing channel 1, push 'utility' and select 'Output Setup'.

View the pulse on a Keysight MSO9404A Infiniium oscilloscope.

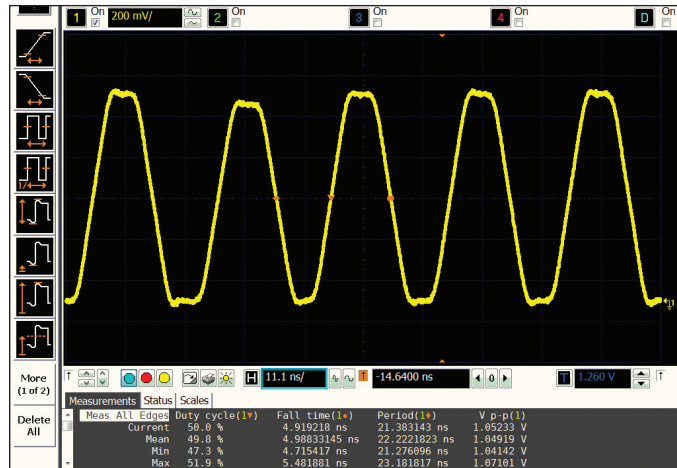


Figure 12. Step 9.

**STEP 10.** Vary the channel 2 delay and level to jitter the pulse.

**STEP 11.** View the jittered pulses on a Keysight MSO9404A Infiniium oscilloscope.

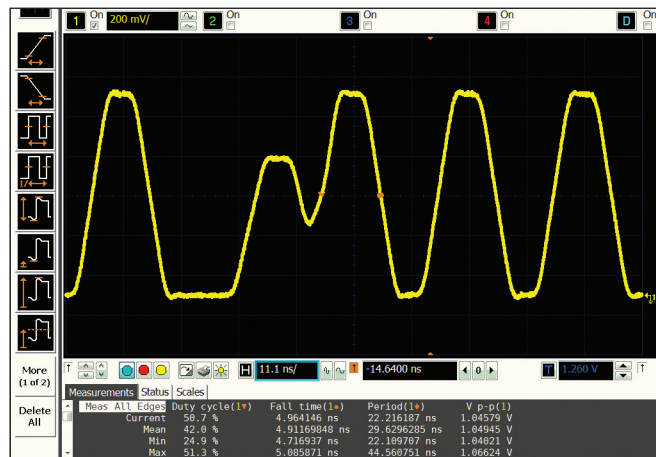


Figure 13. Steps 10 and 11.

## Related Literature

- 81100 Family of Pulse/Pattern Generators** – Brochure
- 81150A and 81160A Pulse Function Arbitrary Noise Generators** – Data Sheet Version 1.1
- 81100 Family of Pulse Pattern Generators Data Sheet** – Version 1.3 – Data Sheet
- Radar Distance Test to Airborne Planes** – Application Note
- Dual Clock Gbit Chip Test** – Application Note
- Magneto-Optical Disk Drive Research** – Application Note
- Simulation of Jittered Synchronization Signals for Video Interfaces** – Application Note
- Radar Distance Test to Airborne Planes** – Technical Overview Version 2
- Dual Clock Gbit Chip Test** – Technical Overview

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