Selecting a Signal Generator for Testing AD Converters

Application Note

Products:

- R&S®SMA100A
- R&S®SMB100A
- R&S®SMC100A

Analog-to-digital converters (ADCs) have taken giant steps in speed over the past decade: Sampling rates of 250 mega-samples per second at 16-bit resolution are now commonplace. Such devices allow high-speed video processing and even software defined radio (SDR) applications, where digitization is being performed at ever-higher intermediate frequencies (IF). This has clearly raised the bar for ADC test equipment, especially regarding the noise performance of the analog input signal and sample clock sources used in the test setup. Since the price of a signal source rises with performance, carefully selecting a generator with the most suitable specifications has become worthwhile if not mandatory.

ROHDE&SCHWARZ

Application Note

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1 Introduction

Many performance parameters for analog-to-digital converters (ADC) are identical to those for analog circuits in general. These include the well-known signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), signal including noise-and-distortion (SINAD), total harmonic distortion (THD) and third-order input intercept (TOII).

A standard test setup to determine the performance of an ADC requires two signal sources, a power supply, preferably one or two bandpass filters and data analysis software. The data analysis software can usually be obtained from the ADC manufacturer. To minimize measurement error, the specifications of the signal sources must always exceed those of the ADC itself.

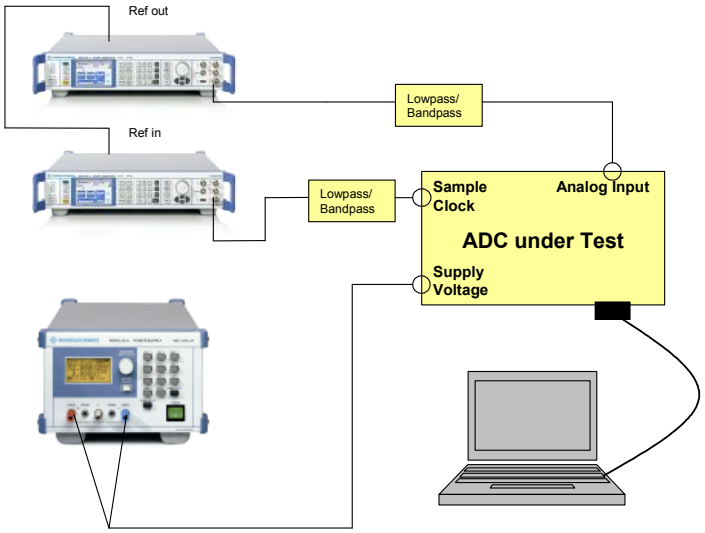

Fig. 1: Typical ADC performance test setup.

In the era when ADCs had a maximum sampling rate of 20 megasamples per second (MSPS) and 50 dB SNR (8-bit resolution), finding a source was no problem since virtually any functional generator surpassed this SNR requirement.

However, the situation has changed considerably over the past decade, and 16 bits at 250 MSPS has become commonplace. Now with high-performance ADC SNR of more than 80 dB, a function or signal generator with an SNR of greater than 90 dB is required. As maximum ADC requirements are quickly approaching the limits of today's high-end signal generators, so it is essential for design and test engineers to know which generator is best suited for testing a specific ADC.

This document outlines the most important aspects concerning ADCs and presents some typical performance data such as jitter and SNR for the analog high-end signal generator R&S®SMA100A when used as a signal source. The appendix provides performance characteristics for other modern analog signal generators from Rohde & Schwarz — the R&S®SMB100A and the R&S®SMC100A — to give the ADC engineer a choice when selecting the most suitable instrument for a particular ADC performance test.

2 Fundamentals

This chapter examines some fundamental aspects and relations concerning ADCs.

2.1 Ideal Signal-to-Noise Ratio (SNR in dB)

- Signal-to-noise ratio (SNR in dB)

  The signal-to-noise ratio (SNR) is the ratio of the RMS signal amplitude to the RMS value of the sum of all spectral components except the first six harmonics and DC. As the input level is decreased, SNR typically decreases decibel-for-decibel in a linear fashion.

For an ideal ADC, the SNR is determined by the quantization noise of the converter and can be calculated as:

$$SNR = 20\log_{10}(\sqrt{1.5}\cdot 2^{n}) \approx 6.02\cdot n + 1.76\,dB \qquad (1)$$

where:

n number of bits.

The ideal SNR for typical ADC resolutions is provided in Table 1.

Number of bits	8	10	12	14	16
SNR/dB	50	62	74	86	98

Table 1: SNR vs. number of bits

For oversampled systems, where the sampling frequency is higher than twice the Nyquist band and with adequate filtering after AD conversion, the SNR must be calculated as:

$$SNR = 20\log_{10}\left(\sqrt{3}\cdot 2^{n-1}\cdot\sqrt{\frac{f_{clk}}{f_{ana\log}}}\right) \qquad (2)$$

$$SNR \approx 6.02\cdot n + 1.76\,dB + 10\log_{10}\left(\frac{f_{clk}}{2\cdot f_{ana\log}}\right) \qquad (3)$$

where:

f_{clk} sampling or clock frequency
f_{analog} analog input frequency

A detailed derivation for equations (1) and (2) can be found in [1].

Undersampling: Today, there is a trend to shift analog-to-digital conversion further forward in the receiver chain, and there are many applications where the IF signal is converted to the digital domain. The IF of an analog TV, for instance, is approx. 40 MHz. This signal is usually downconverted by the ADC via a technique called undersampling, where sampling does not take place at 81 MSPS but, instead, with a much lower frequency. Undersampling has a major impact on determining the specifications of the sample clock generator used in the test setup as illustrated later (see section 2.7).

2.2 Jitter

Jitter is one of the most critical parameters when discussing the SNR performance of a real ADC. It describes the stability of a signal in the time domain and specifies the signal's fluctuations of zero crossing as shown in Fig. 2 for a 10 MHz sine signal with very high jitter (yellow trace $t_{jitter1}$) and low jitter (blue trace $t_{jitter2}$).

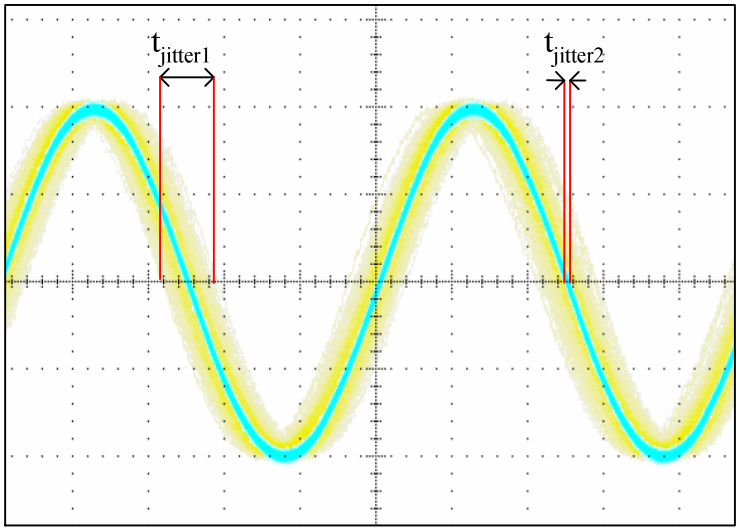

Fig. 2: 10 MHz signal with very high jitter (yellow trace) and with low jitter (blue).

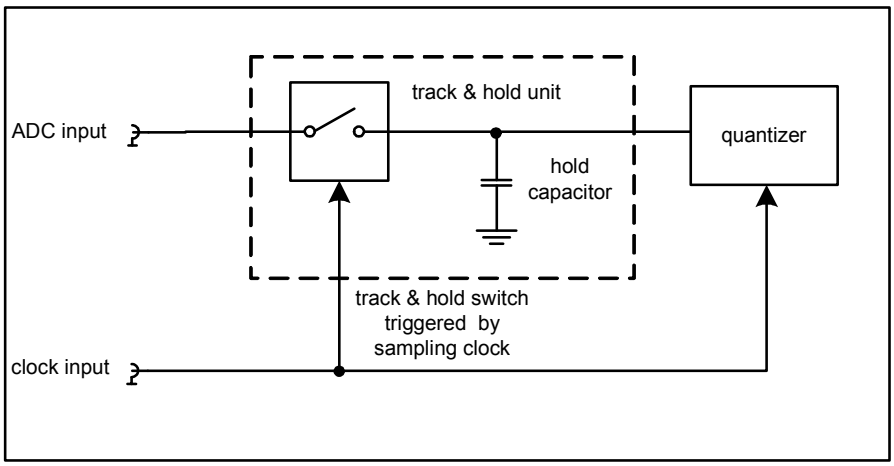

Fig. 3: Basic block diagram of track & hold unit of an ADC input stage.

Fig. 3 is a basic block diagram of the track & hold unit of an ADC input stage. At the beginning of the sampling process, the track & hold switch is closed and the voltage at the hold capacitor follows the input voltage. The zero crossing of the ADC's clock signal opens the track & hold switch, and the voltage across the capacitor is held. The conversion process in the quantizer is then performed. Any error in the zero crossing point will therefore translate to a voltage error at the hold capacitor. The voltage error is proportional to the jitter and input slope of the signal as shown in Fig. 4 below:

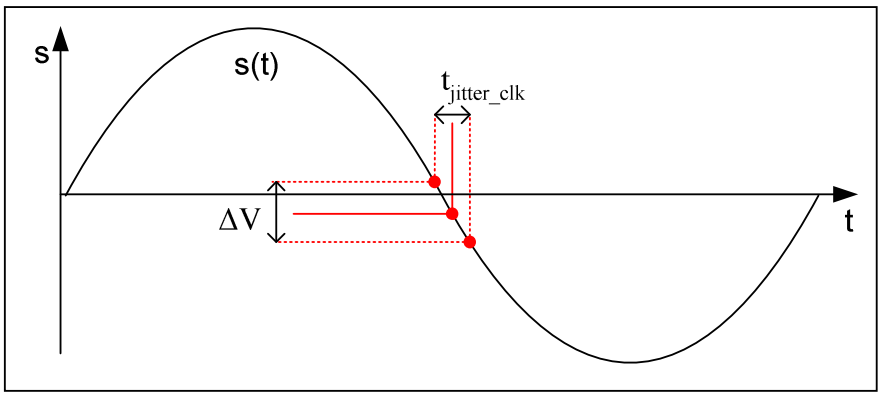

Fig. 4: Voltage error ΔV due to jitter on sampling clock (t_{jitter_clk}).

The voltage error ΔV of signal s(t) due to sampling jitter in Fig. 4 can be expressed as:

$$\Delta V = slewrate\big(s(t)\big) \cdot t_{jitter} = \frac{d}{dt} s(t) \cdot t_{jitter\_clk} \quad (4)$$

For a sine wave signal, s(t) is determined as follows:

$$s(t) = A \cdot \sin\left(2\pi \cdot f_{ana\log} \cdot t\right) \quad (5)$$

The slew rate is determined by differentiating equation (5) as

$$\frac{d}{dt} s(t) = A \cdot 2\pi \cdot f_{ana\log} \cdot \cos\left(2\pi \cdot f_{ana\log} \cdot t\right) \quad (6)$$

Substituting (6) in equation (4) yields the voltage error ΔV:

$$\Delta V = A \cdot 2\pi \cdot f_{ana\log} \cdot t_{jitter} \cdot \cos\left(2\pi \cdot f_{ana\log} \cdot t\right) \quad (7)$$

The RMS value for the voltage error ΔV can be expressed as:

$$\Delta V_{RMS} = \sqrt{\frac{1}{T} \cdot \int_0^T \Delta V(t)^2 \, dt} = \frac{A}{\sqrt{2}} \cdot 2\pi \cdot f_{ana\log} \cdot t_{jitter\_clk} \quad (8)$$

The SNR due to clock jitter can be calculated as the relation between the RMS signal voltage and the RMS voltage error:

$$SNR_{jitter\_clk} = 20\log\left(\frac{\frac{A}{\sqrt{2}}}{\frac{A}{\sqrt{2}} \cdot 2\pi \cdot f_{ana\log} \cdot t_{jitter\_clk}}\right) = \quad (9)$$

$$SNR_{jitter\_clk} = -20\log\left(2\pi \cdot f_{ana\log} \cdot t_{jitter\_clk}\right) \quad (10)$$

where:

f_{analog}	analog input frequency to the ADC
t_{jitter_clk}	RMS clock jitter

The RMS jitter of a signal is the most commonly used expression, and it is normally used for SNR calculation. If a signal with a Gaussian-distributed jitter is considered, the RMS value for the jitter is determined using the standard deviation.

For signals where jitter is generated by a sinusoidal modulation, e.g. if a discrete spurious tone dominates the jitter performance, the peak-to-peak jitter can be expressed as:

$$Jitter_{Peak-Peak\_spur} = Jitter_{rms\_spur} \cdot 2 \cdot \sqrt{2} \quad (11)$$

where:

$Jitter_{rms\_spur}$	RMS jitter generated by a discrete spurious non-harmonic (see equation (26) below)

For some digital data transmission standards working with different data rates (e.g. SONET/SDH), the *unit interval* (UI) jitter is normally used instead of the RMS jitter. This allows a consistent comparison of jitter for different data rates.

The UI jitter relates the RMS jitter value to the cycle duration of the signal and is calculated by dividing the RMS jitter by the signal period (or by multiplying by the signal frequency):

$$Jitter_{UI} = Jitter_{rms} / T_o = Jitter_{rms} \cdot f_o \quad (12)$$

where:

T_o	signal period
f_o	signal frequency

2.3 Relation between Phase Noise and Jitter

Generally, the noise performance of signal generators is specified as single sideband phase noise (SSB phase noise $L(f_{off})$), as shown in Fig. 5 for the R&S®SMA100A at 125 MHz.

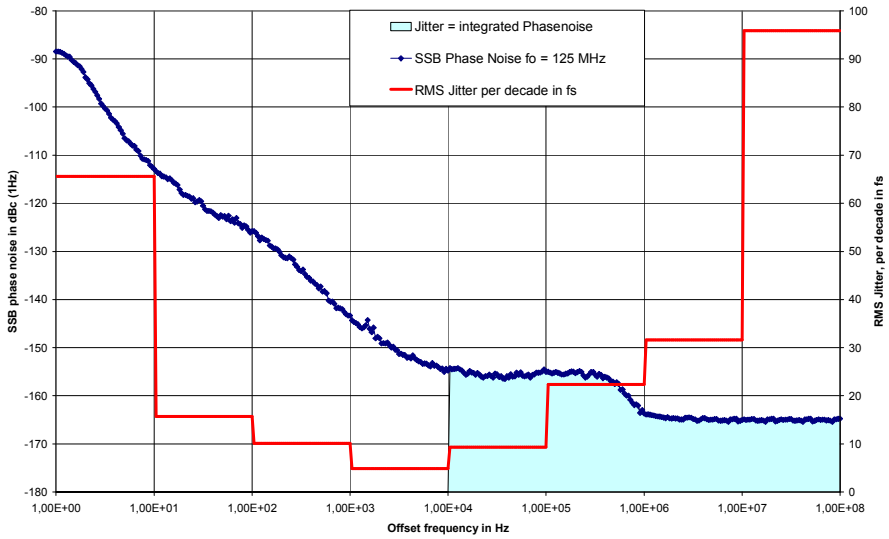

Fig. 5: SSB phase noise and RMS jitter measured using the R&S®SMA100A with option -B22.

The SSB phase noise $L(f_{off})$ is defined as the ratio of the spectral power density in 1 Hz bandwidth at a carrier offset f_{off} to the carrier power. The SSB phase noise describes the signal quality of a signal source in the frequency domain.
Since there is a direct relationship between phase noise and jitter, it is possible to relate one to the other. RMS jitter is evaluated by integrating the phase noise within a defined bandwidth, as graphically illustrated by the blue area in Fig. 5 for a bandwidth from 10 kHz to 100 MHz. RMS jitter can be calculated from the SSB phase noise as shown:

$$t_{jitter} = \frac{1}{2\pi f_o}\sqrt{2 \cdot \int_{f_1}^{f_2} 10^{\frac{L(f_{off})}{10}}\, df_{off}} \qquad (13)$$

where:

f_o	carrier frequency
f_1	lower offset frequency for integration
f_2	upper offset frequency for integration
$L(f_{off})$	single sideband phase noise at offset f_{off}

The integral in equation (13) is multiplied with a factor of 2 in order to consider both sidebands of the single sideband phase noise.

In Fig. 5, the RMS jitter for the SSB phase noise is calculated for each decade and plotted as the red trace. As the figure clearly shows, the jitter contribution close to the carrier rises since the phase noise increases very rapidly in this area. But a question remains: Why does the jitter per decade increase again for offsets above 100 kHz while the phase noise decreases in this area? The reason is the increasing integration bandwidth used for the jitter calculation. For example, the bandwidth for jitter calculation from 1 MHz to 10 MHz is 9 MHz as compared to 90 kHz for the decade from 10 kHz to 100 kHz. For this example, the integration bandwidth has increased by a factor of 100 (= 20 dB) whereas the phase noise contribution is only approx. 10 dB lower.

Since frequency offsets close to the carrier are of no consequence to high speed applications (see also section 2.4 Jitter Bandwidth), it is clear that wideband noise is the most significant parameter affecting jitter performance for high-speed ADCs.

If the total jitter contribution for multiple decades is needed, it is necessary to take the root sum square of the individual jitter contributors per decade.

2.4 Jitter Bandwidth

One important aspect when calculating jitter is the bandwidth (difference in offset frequencies f_1 and f_2 in equation (13)), which should be considered for integration. The lower offset frequency f_1 depends on the frequency resolution (or in other words, the observation time for one FFT shot) of the system under consideration and can be calculated as:

$$f_1 = \frac{f_{clk}}{FFT\ length} \tag{14}$$

where:

f_{clk}	clock or sampling frequency of the ADC
FFT length	number of FFT samples, e.g. 65536 for a 64k FFT

Example: A 64k FFT performed with an ADC running at 80 MSPS encode rate leads to a frequency resolution of:

$$f_1 = \frac{80\ MHz}{65536} = \quad 1221\ Hz$$

This example demonstrates that for most high-speed ADC applications, the phase noise close to the carrier does not matter because phase fluctuations that are slower than the measurement time for one FFT bin do not add to the measurement result. The phase noise close to the carrier is more dominant in systems with high frequency resolution and thus long sampling periods.

The upper offset frequency f_2 depends on the maximum signal bandwidth and is normally different for the analog and the clock paths. The analog input bandwidth usually equals the Nyquist band ($f_{clk}/2$), but could be much lower for narrowband applications. The bandwidth of the clock path depends on the filtering used and can range from several MHz up to a few GHz. Since equation (13) performs the integration for both sidebands of SSB phase noise, the upper offset frequency f_2 is always half the signal bandwidth.

Example: For an ADC running at 125 MSPS encode rate and a clock bandwidth of 200 MHz, the upper offset frequency for jitter calculation is 100 MHz.

Regardless of jitter bandwidth, the lowest possible jitter – and therefore the best SNR – can only be achieved by using proper filtering on both the analog input and clock paths.

One important aspect needs to be mentioned here: Since an ADC is a sampled system, the analog input signal is convolved with the clock signal in the frequency domain. This means that the spectral distribution of the clock signal shapes the analog signal at the ADC output. If the bandwidth of the clock signal is greater than the Nyquist band, the wideband noise of the clock signal will be aliased completely into the Nyquist band as graphically shown in Fig. 6.

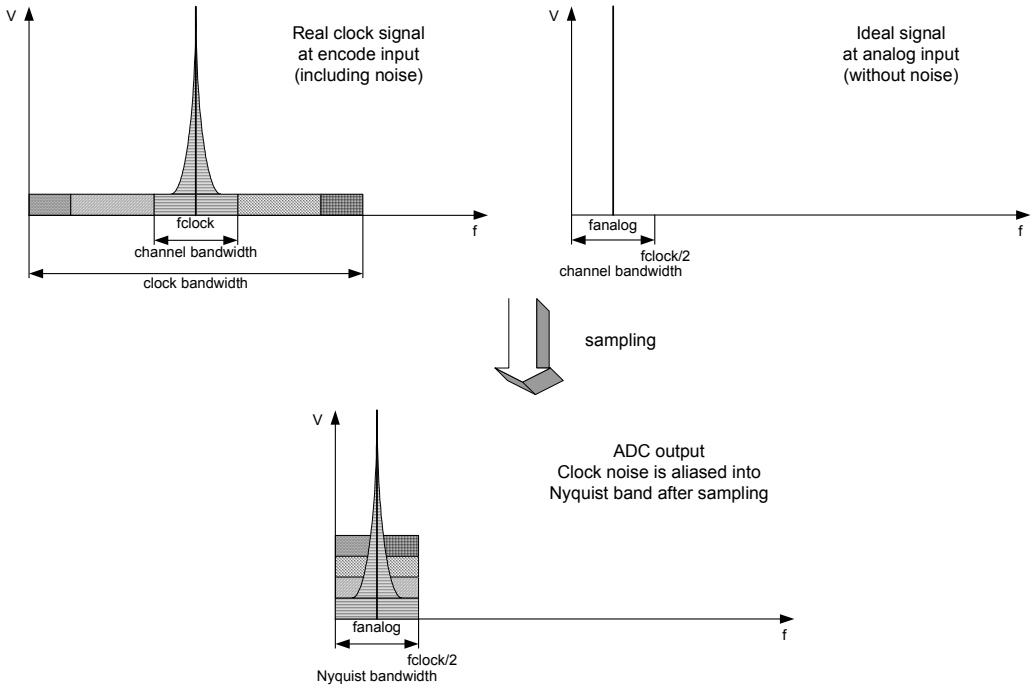

Fig. 6: Graphical illustration of clock noise aliasing into Nyquist band.

As a result, the energy of the clock signal's wideband noise is accumulated many times within the Nyquist band, thus reducing the SNR significantly.

Example: For an ADC running at a clock rate of 80 MSPS and a clock bandwidth of 160 MHz, the wideband noise of the clock signal is aliased 4 times into the Nyquist band (40 MHz), causing a degradation of the SNR contribution due to the clock source of 6 dB.

2.5 Real Signal-to-Noise Ratio (SNR in dB)

The SNR of a real ADC is degraded from the values provided above, and it is illustrated for a typical 14-bit ADC in Fig. 7 below.

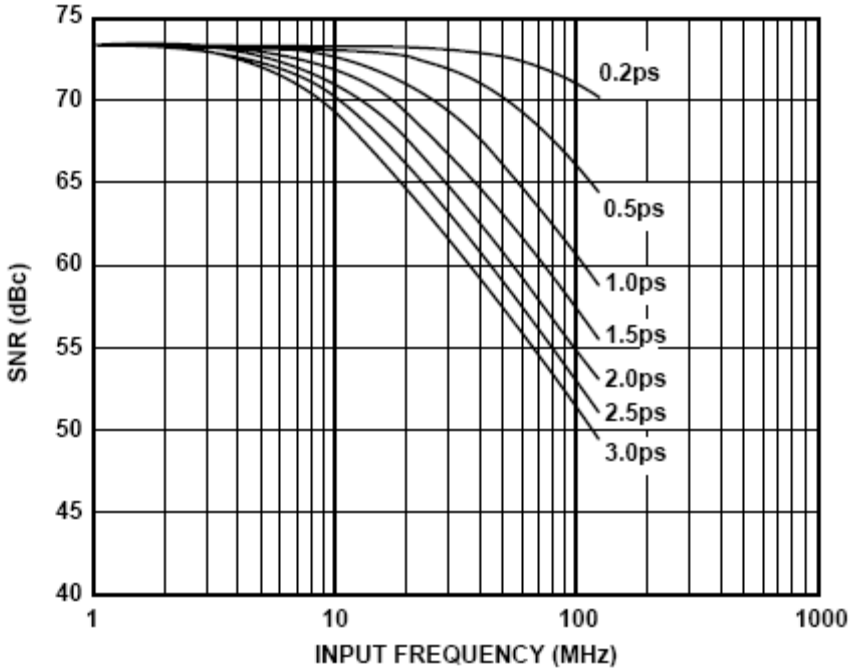

Fig. 7: ***SNR vs. analog input frequency and clock jitter [6].***

Fig. 7 shows that for a real 14-bit converter, it is not possible to reach the ideal SNR of 86 dB even at very low input frequencies. This is due to factors such as jitter on the clock and analog input signals as well as factors associated with ADC design, including intrinsic aperture jitter, differential nonlinearities (DNL) in the ADC quantizer and other internal noise such as thermal noise.

The real signal-to-noise ratio due to these effects can be calculated as:

$$SNR_{ADC\_real} = -10\log_{10}\left(10^{-SNR_{ADC\_Noise}/10} + 10^{-SNR_{jitter}/10}\right) \quad (15)$$

with

$$SNR_{ADC\_Noise} = -20\log_{10}\sqrt{\left(\frac{U_{thermal}}{2^n}\right)^2 + \left(\frac{1+e}{2^n}\right)^2} \quad (16)$$

and

$$SNR_{jitter} = -20\log_{10}\sqrt{(2\pi f_{ana\log})^2 \cdot \left(t^2_{jitter\_ADC} + t^2_{jitter\_clk} + t^2_{jitter\_ana}\right)} \quad (17)$$

where:

SNR_{ADC_Noise}	signal-to-noise contribution due to ADC noise and nonlinearities
SNR_{jitter}	signal-to-noise contribution due to jitter
$U_{thermal}$	internal thermal noise of the converter
n	number of bits
e	average differential nonlinearity (DNL) of converter
f_{analog}	analog input frequency
t_{jitter_ADC}	intrinsic aperture RMS jitter of the converter
t_{jitter_clk}	RMS jitter of the clock source
t_{jitter_ana}	RMS jitter of the analog signal source

Equation (16) describes the device's intrinsic noise floor due to thermal noise and converter nonlinearities. This noise floor is constant over input frequency and can therefore be neglected at high signal frequencies, where SNR degradation due to jitter becomes dominant. However, at low input frequencies, these effects determine the maximum available SNR, e.g. 73 dB for the ADC shown in Fig. 7.

At higher frequencies, the SNR performance of a converter is mainly determined by jitter as seen in the set of curves in Fig. 7. Equation (17) provides the mathematical description for the SNR performance of an ADC due to jitter and shows that the impact of jitter increases with higher signal input frequency.

Substituting (16) and (17) into equation (15) yields:

$$SNR_{ADC\_real} = -20\log_{10}\sqrt{(2\pi f_{ana}\log t_{jitter})^2 + \left(\frac{U_{thermal}}{2^n}\right)^2 + \left(\frac{1+e}{2^n}\right)^2} \quad (18)$$

where

t_{jitter} RMS sum of all jitter contributions

$$t_{jitter} = \sqrt{t_{jitter\_clk}^{\ 2} + t_{jitter\_ana}^{\ 2} + t_{jitter\_ADC}^{\ 2}} \quad (19)$$

or in exponential form

$$SNR_{ADC\_real} = -10\log_{10}\left(10^{-SNR_{ADC\_Noise}/10} + 10^{-SNR_{jitter\_ADC}/10} + 10^{-SNR_{jitter\_clk}/10} + 10^{-SNR_{jitter\_ana}/10}\right) \quad (20)$$

One common way to isolate the SNR contributors of an ADC is to perform an SNR measurement at a specific clock rate with a very low input frequency (yields SNR_{ADC_Noise}) and a second SNR measurement with the same clock rate but at a very high input frequency (yields SNR_{ADC_real}). Using equation (15), the SNR due to jitter can be calculated, but it is not possible to determine which part is from the ADC and which part is from the clock or analog source.
If the jitter contribution of the analog source and clock source is known, it is possible to isolate the ADC jitter using equation (20).

2.6 Relation between Wideband Phase Noise, Jitter and SNR at Clock Input

For most ADCs, the amplitude of the clock signal is hard-limited by the use of internal differential input and buffer stages. This minimizes amplitude effects; therefore, only fluctuations of zero crossings (= phase noise) of the clock signal influence the sampling process.
As already pointed out for most high-speed applications, the close-in phase noise can be neglected. Therefore, only the wideband phase noise of the clock signal contributes to the SNR performance of the ADC. Since for offsets >10 MHz the spectral density of wideband phase noise can be considered as constant and flat over offset frequency, the integration of the spectral noise density for jitter calculation (see equation (13)) can be expressed as:

$$Noise_{\text{int}egrated} = BBNoise_{clk} + 10\log_{10}\left(BW_{clk}\right) \quad (21)$$

where:

$BBNoise_{clk}$	broadband or wideband phase noise of clock signal
BW_{clk}	clock bandwidth

Replacing the integral in equation (13) by equation (21), the clock jitter can be calculated by:

$$t_{jitter\_clk} = \frac{1}{2\pi f_{clk}}\sqrt{10^{Noise_{\text{int}egrated}/10}} \quad (22)$$

The multiplier of 2 for the integral, representing both SSB phase noise sidebands, is already included in $Noise_{integrated}$ in equation (22) since the complete clock bandwidth is used for the integration.

Substituting t_{jitter_clk} in equation (10) by equation (22) yields:

$$SNR_{jitter\_clk} = -20\log_{10}\left(2\pi f_{ana\log}\frac{1}{2\pi f_{clk}}\sqrt{10^{Noise_{\text{int}egrated}/10}}\right)$$

$$SNR_{jitter\_clk} = -Noise_{\text{int}egrated} - 20\log_{10}\left(\frac{f_{ana\log}}{f_{clk}}\right)$$

and substituting $Noise_{integrated}$ by equation (21) yields:

$$SNR_{jitter\_clk} = -BBNoise_{clk} - 10\log_{10}(BW_{clk}) - 20\log_{10}\left(\frac{f_{ana\log}}{f_{clk}}\right) \quad (23)$$

where:

$BBNoise_{clk}$	spectral density of **wideband phase noise** of ADC clock signal
BW_{clk}	bandwidth of ADC clock signal
f_{analog}	analog input frequency of ADC
f_{clk}	clock or sampling frequency of ADC

Equation (23) evaluates the SNR of an ADC in the frequency domain using phase noise spectral density, whereas equation (10) calculates the SNR in the time domain using jitter. Nevertheless, both equations should yield the same result as demonstrated in the following example.
As equation (23) assumes a flat and constant spectral density of phase noise, the calculation is only valid for a high clock bandwidth where the SNR is dominated by wideband phase noise instead of close-to-carrier synthesizer phase noise.

Example: ADC with 125 MSPS clock rate (Nyquist band = 62.5 MHz) and 50 MHz analog input frequency. A 16 k FFT is performed, resulting in a frequency resolution of approx. 8 kHz (→ lower boundary for jitter integration = 10 kHz).
The clock source is the *R&S®SMA100A*, with the phase noise performance shown in Fig. 5.

- Calculation with clock bandwidth BW_{clk} = 200 MHz (f_{clk} ± 100 MHz)

  In this example, the clock noise is aliased more than three times into the Nyquist band.

  Calculation according to equation (10)
  t_{jitter_clk} = 102 fs (jitter bandwidth 10 kHz to 100 MHz)

$$\begin{aligned} SNR_{jitter\_clk} &= -20\log_{10}(2\pi f_{ana\log} t_{jitter\_clk}) \\ &= -20\log_{10}(2\pi \cdot 50MHz \cdot 102\,fs) = 89.9\,dB \end{aligned}$$

  Calculation according to equation (23)
  $BBNoise_{clk}$ = –164.5 dBc(Hz) (see Fig. 5)

$$\begin{aligned} SNR_{jitter\_clk} &= -BBNoise_{clk} - 10\log_{10}(BW_{clk}) - 20\log_{10}\left(\frac{f_{ana\log}}{f_{clk}}\right) \\ &= 164.5dBc - 10\log_{10}(200MHz) - 20\log_{10}\left(\frac{50MHz}{125MHz}\right) = \quad 89.5\,dB \end{aligned}$$

  Both results are within half of a dB and coincide very well.

- Calculation with clock bandwidth BW_{clk} = 20 MHz (f_{clk} ± 10 MHz):

  In this example, the clock noise is convolved into the Nyquist band only one time.

  Calculation according to equation (10)
  t_{jitter_clk} = 38.6 fs (jitter bandwidth 10 kHz to 10 MHz)

$$\begin{aligned} SNR_{jitter\_clk} &= -20\log_{10}(2\pi f_{ana\log} t_{jitter\_clk}) \\ &= -20\log_{10}(2\pi \cdot 50MHz \cdot 38.6\,fs) = 98.3\,dB \end{aligned}$$

  Calculation according to equation (23)
  $BBNoise_{clk}$ = -164.5 dBc(Hz) (see Fig. 5)

$$\begin{aligned} SNR_{jitter\_clk} &= -BBNoise_{clk} - 10\log_{10}(BW_{clk}) - 20\log_{10}\left(\frac{f_{ana\log}}{f_{clk}}\right) \\ &= 164.5dBc - 10\log_{10}(20MHz) - 20\log_{10}\left(\frac{50MHz}{125MHz}\right) = \quad 99.5\,dB \end{aligned}$$

  The two results differ more than 1 dB because the assumption of a flat noise distribution for the spectral calculation is slightly too optimistic, as the influence of the increased phase noise below 1 MHz is not taken into account. However, the contribution to the SNR of these spectral components becomes more influential at lower clock bandwidths.

2.7 Effects in Under- or Oversampled Systems

More and more modern communication systems are implementing direct conversion of high IF frequencies into the digital domain. To support lower clock frequencies, a technique called undersampling is used. It means that the sampling rate is lower than the signal frequency. However, the spectral purity requirements of the clock signal that is used are considerably higher in such systems as shown below.
An important factor here is the last term of the equation (23):

$$-20 \cdot \log\left(f_{ana\log} / f_{clk}\right)$$

It reveals that the SNR of a sampled system depends on the relation of signal frequency to clock rate and that the SNR degrades 6 dB every time the analog input frequency is doubled.
The reason can easily be understood by graphically displaying the effect of jitter for both oversampling and undersampling. In the case of undersampling, the slightest delay in sampling generates a huge variation in the sampled value. This is depicted below.

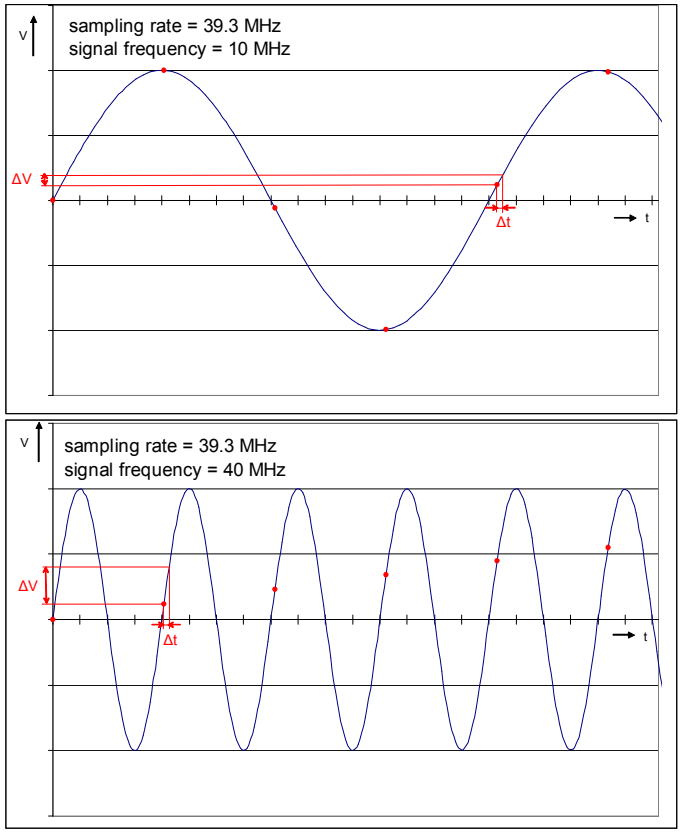

Fig. 8: Effect of jitter on over- and undersampled systems.

In contrast, oversampled systems — where the clock rate is much higher than the signal frequency — use this relation to reduce the noise contribution of the clock source.

This is an important element for ADCs used in undersampled IF stage systems since the *S/N* ratio can deteriorate considerably. It is absolutely necessary to verify whether the performance of the clock source is in compliance with the required specification. The requirements for the phase noise of the clock source in undersampled systems are much higher than in baseband systems. The performance in many IF-sampling radio architectures is limited by clock phase noise, not data converter performance.

Fig. 9 illustrates the effect on SNR vs. ratio f_{analog}/f_{clk}:

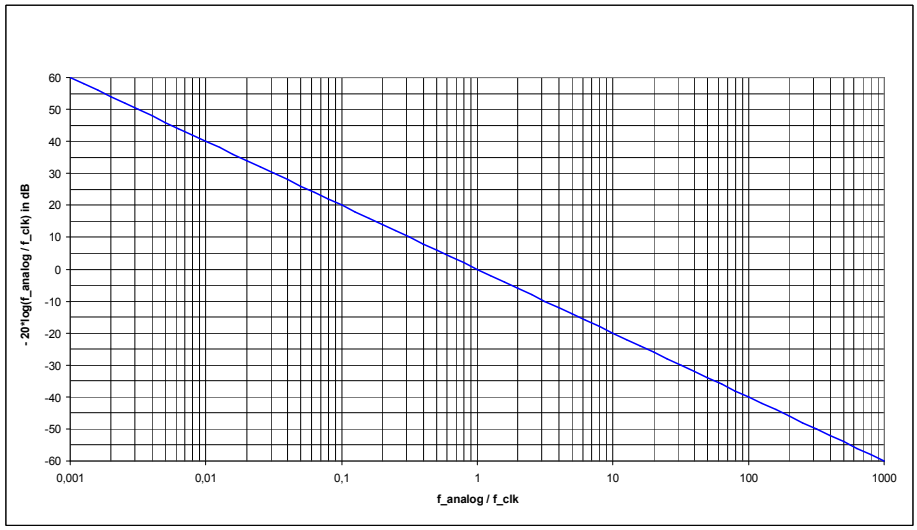

Fig. 9: Effect on SNR vs. ratio f_{analog}/f_{clk}.

2.8 Relation between Wideband Noise, Jitter and SNR at Analog Input

Any calculation of the SNR contribution of an ADC's analog signal input must take the amplitude and phase noise of the analog signal source into account since no amplitude-limiting input stages are present at the analog input — in contrast to the clock input.
Equation (23) describes the SNR due to phase noise at the clock input. For the analog signal input, the relation must be changed to:

$$SNR_{ana\log} = -BBNoise_{ana\log} - 10\log_{10}\left(BW_{ana\log}\right) \quad (24)$$

where:

$BBNoise_{analog}$	spectral density of the **overall wideband noise** of the ADC analog input signal. It is the sum of phase noise and amplitude noise. In the case of white noise, which is assumed for offset frequencies >10 MHz, the amplitude and phase noise contributions are equal and uniformly distributed. Therefore, the overall wideband noise is normally 3 dB higher than the wideband phase noise.
BW_{analog}	bandwidth of the ADC analog input signal (normally fclk/2)

Since equation (24) assumes a flat and constant spectral density of wideband noise, the calculation is only valid for a high analog bandwidth where SNR is dominated by wideband noise instead of close-to-carrier synthesizer phase noise.

Equation (24) also shows that the relation between clock rate and analog signal frequency has no effect on the SNR contribution of the analog signal source to ADC performance.

2.9 Distortion and Spurious

Besides noise performance, the spectral purity due to spurious and signal distortion is the most important parameter of an ADC.
Definitions of some commonly used expressions are listed below:

- **Signal-to-noise and distortion (SINAD in dB)**

  The signal-to-noise and distortion (SINAD) value is the ratio of the RMS signal amplitude to the RMS level of the sum of all spectral components, including harmonics but excluding DC. The difference between SNR and SINAD is the energy contained in the first six harmonics.

- **Total harmonic distortion (THD in dBc)**

  Total harmonic distortion (THD) is the ratio of the RMS signal energy to the RMS value of the sum of the first six harmonics.

- **Spurious-free dynamic range (SFDR)**

  The spurious-free dynamic range (SFDR) is the ratio of the RMS level of the signal to the RMS level of the peak spurious spectral component at the ADC output that produces the worst result. In most cases, SFDR is determined by a harmonic of the analog input signal applied to the ADC.

To measure these parameters, an analog signal source with very low harmonic distortion and non-harmonics is required.

- **Third-order input intercept point (IIP3 in dBm)**

  The third-order input intercept point (IIP3) is determined by applying a two-tone signal to the analog input of the ADC, thus yielding an extrapolated input level at which the level of the intermodulation distortion products and the analog input signal converge.
  The IIP3 is normally far beyond the maximum input level of the analog input, but it is a measure of the linearity of the ADC’s input stage.

2.9.1 Harmonics

Harmonics are integer multiples of the fundamental signal frequency that are generated at each amplifier stage within the RF path due to semiconductor nonlinearities. The offset frequency to the carrier can be evaluated exactly, and it makes the use of suitable filters for suppression possible.
Generally, the signal generator's harmonic distortion is less critical than the non-harmonic performance since the frequencies of the harmonic spurs are known (integer multiple of the fundamental signal) and since these spurs are located far from the carrier in the case of most high-speed applications.
Harmonics applied to the ADC's clock input normally do not influence the performance of the converter since the zero crossing of the clock signal is not shifted by harmonic signal components. Furthermore, the ADC's clock input stage normally converts an applied sine signal into a square signal containing strong harmonic signal components.
For the analog input signal, harmonic distortion is very critical to ADC performance; therefore, proper filtering of the input signal is essential. This filtering is required because the performance of the signal generator is naturally considerably worse than the performance of an ADC. Spur filtering can be performed with lowpass or bandpass filters, i.e. a typical harmonic suppression of 30 dBc to 40 dBc is normally sufficient for the signal source in most applications.

Lowpass filters suppress the harmonics effectively and have the advantage that the frequency of the source signal can still be varied across a specific range. However, part of the wideband noise is still passed to the ADC and the noise contribution of the analog signal source can only be improved partially.

Bandpass filters have an identical effect on the harmonics, but they also have the additional advantage that the noise and subharmonics are suppressed more effectively. The disadvantage is that the test can only take place within a narrow frequency range, so several filters are needed in order to perform tests over a wide frequency range.

For both filter types, the high frequency suppression of the used filter must be examined carefully in order to eliminate high-order harmonics of the input signal. This signal could possibly cross the clock frequency, or even a multiple of it and could alias back to the Nyquist band. If more than one filter is used consecutively, a fixed attenuator between the filters should be used to improve the matching between these filters. Otherwise, the filter characteristic may become much worse than expected.

Example: Assume that an ADC is running at a clock rate of 1 GSPS and that the analog input frequency is 428 MHz. Due to insufficient filtering, the 6th harmonic of the input signal at 2568 MHz is only suppressed by 5 dB. Therefore, it is applied with a level of, for example, –90 dBc (relative to the fundamental) to the input of the converter. As a result, an alias product as shown in the following might appear in the output spectrum of the converter:

$$f_{alias} = (3 \cdot f_{clk}) - (6 \cdot f_{analog}) = 432 \text{ MHz}$$

2.9.2 Non-Harmonics

For signal generators, non-harmonic signal components are more critical than harmonics because adequate filtering is normally not possible. The frequency of a non-harmonic spurious cannot be predicted, which means that the offset to the carrier is unknown. A spurious line can appear very close to the carrier (e.g. 20 kHz) for one frequency and very far from the carrier (e.g. 100 MHz) at another frequency.
Non-harmonics are critical to both the clock and the analog signal input of an ADC because a non-harmonic normally modulates the phase of a signal and thus the zero crossing of the clock signal at the ADC input stage is varied.
For a spurious at the clock input, the level of this non-harmonic at the ADC output signal depends on the relation between the clock and analog signal frequency, just like for the phase noise of the clock signal. Therefore, the spur level of the clock signal must be corrected by the following expression:

$$k = 20 \cdot \log\left(f_{ana\log} / f_{clk} \right) \tag{25}$$

Example: A spur at –80 dBc is present at the clock signal of an ADC running with 20 MSPS clock rate and an analog input frequency of 50 MHz. According to equation (25), the spurious appears at the converter output at a level of -72 dBc, reducing the SFDR performance of the ADC drastically.

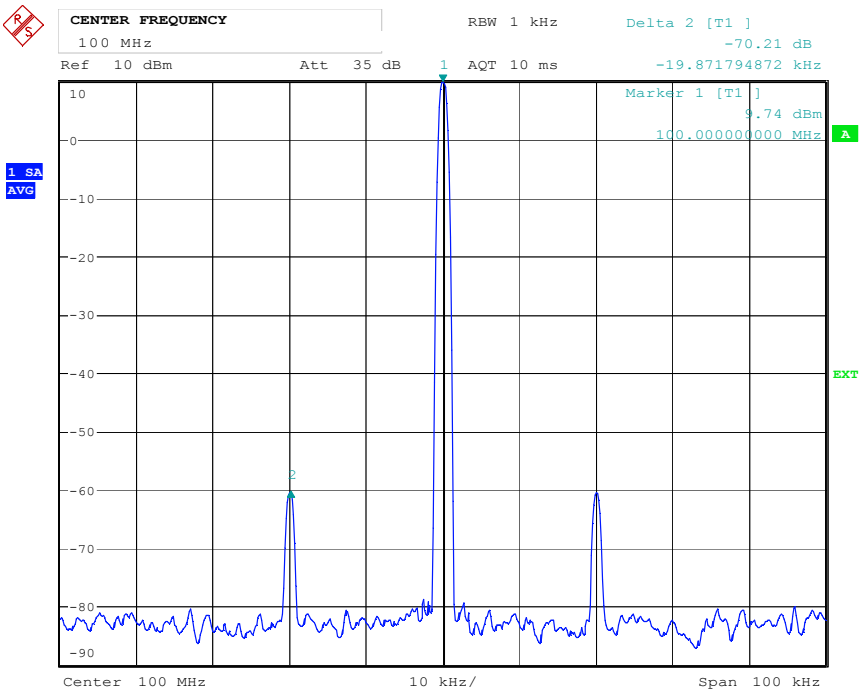

Fig. 10: ***Symmetrical pair of non-harmonic spurs at 20 kHz carrier offset.***

Fig. 10 shows a symmetrical pair of spurs for a 100 MHz carrier frequency at 20 kHz offset generated by a low-performance signal source with a (single sideband) spur level of -70.2 dBc. Since the spur phase-modulates the carrier, the spectrum shows two symmetrical non-harmonics with the same level on both sides of the carrier. If the spectrum of a non-harmonic shows different levels for the left- and right-hand spurs, the amplitude of the carrier is also modulated with the same frequency.

The level of a non-harmonic spur is normally independent from the output level of the signal generator since most non-harmonics phase-modulate the carrier. Thus, the level of the spurious signal generally changes in proportion to the carrier frequency, resulting in a spur level degradation of 6 dB if the carrier frequency is doubled and a spur level improvement of 6 dB if the carrier frequency is halved by using a frequency divider. This relation is not valid for signals generated by mixing instead of dividing, which is an important fact when generating low frequencies.

There are two competing concepts for generating low frequencies. The conventional design uses a mixer to downconvert a high frequency signal to a low frequency. It is normally used in vector signal generators such as the *R&S®SMU200A* or *R&S®SMBV100A* since it is not possible to downconvert an IQ-modulated signal by using a frequency divider. An important drawback of this concept is the reduced spectral purity of the low frequency signal, because the spurious components of the high frequency signal are directly converted to the low frequency signal and additional mixing spurs may occur.

A divider concept is normally the preferred solution for an analog signal generator such as the *R&S®SMA100A* or *R&S®SMB100A: S*ignal performance with regard to wideband noise and non-harmonics is much better than compared with the mixer design, and there are no limitations due to IQ-modulated signals. For carrier frequencies generated by division of the fundamental synthesizer octave (e.g. 750 MHz to 1500 MHz), the levels of all synthesizer non-harmonics are decreased by the division factor. For example, for a 10 MHz output signal generated by dividing a 1280 MHz signal by 128, all synthesizer spurs are reduced by 42 dB. The *R&S®SMA100A* signal generator uses such a divider concept for generating low frequencies, and therefore provides extremely low non-harmonics of typ. <100 dBc for frequencies below 750 MHz.

When selecting an appropriate signal source for ADC testing, the spurious specification of the source must be carefully considered over the complete frequency range. As a first approach, the performance of the signal source should be approx. 10 dB better than the performance of the tested DUT.

If the non-harmonic performance of a signal generator has to be verified by using a spectrum analyzer, it is not possible to distinguish whether a spur is generated by the signal generator or the spectrum analyzer. One often used procedure to exclude the influence of the spectrum analyzer is to change the settings of the analyzer (e.g. center frequency, input attenuation, filter type) and observe the spur level. If the spur level is varying, the signal generator is normally not the source for this spur. Another way to verify the analyzer's performance is to apply exactly the same signal (frequency and level) from a completely different signal source (e.g. the *R&S® SMB100A* instead of the *R&S® SMA100A*) to the analyzer and check the spur level. If the spur level is not varying, the non-harmonic may possibly be generated from the spectrum analyzer.

2.9.2.1 Relation between Non-Harmonics and Jitter

Due to the phase modulation of non-harmonics, the RMS jitter of the signal is also influenced and can be calculated as follows for a sinusoidal phase modulating spurious:

$$t_{jitter\_rms} = \frac{\Delta\varphi_{rms}}{\omega_o} = \frac{\frac{1}{\sqrt{2}} \cdot 2 \cdot 10^{\left(\frac{a\_spur}{20}\right)}}{2 \cdot \pi \cdot f_o} = \frac{10^{\left(\frac{a\_spur}{20}\right)}}{\sqrt{2} \cdot \pi \cdot f_o} \quad (26)$$

where:

a_spur	the (single sideband) level of a non-harmonic pair of spur related to the carrier level in dBc
f_o	the carrier frequency

If more than one symmetrical pair of spurs are present in the signal, the SNR is deteriorated by

$$SNR_{m \cdot spur} = -10\log_{10}\left(\sum_{n=1}^{m} 10^{-SNR_{spur\_n}/10}\right) \quad (27)$$

where:

SNR_{spur_n}	the SNR contribution of one symmetrical non-harmonic pair of spurs in dB
m	the total number of pairs of spurs contained in the signal

2.9.2.2 Relation between Non-Harmonics and SNR

The SNR contribution of a non-harmonic at the clock input of an ADC can be calculated by substituting equation (26) in equation (10).

$$SNR_{spur\_clock} = -20\log\left(\frac{10^{\frac{a\_spur_{clock}}{20}} \cdot 2 \cdot \pi \cdot f_{ana\log}}{\sqrt{2} \cdot \pi \cdot f_{clk}}\right)$$

$$SNR_{spur\_clock} = -a\_spur_{clock} - 3dB - 20\log\left(\frac{f_{ana\log}}{f_{clock}}\right) \quad (28)$$

For a spur at the analog input of an ADC, equation (27) simplifies to

$$SNR_{spur\_ana\log} = -a\_spur_{ana\log} - 3dB \quad (29)$$

2.9.2.3 Relation between Non-Harmonics and SFDR

The SFDR due to a non-harmonic spurious at the analog signal input of an ADC is equal to the spurious distance of the signal source.
The sign is different since the spurious distance is the relation of spur level to signal level, and SFDR is the ratio of signal level to spur level.

For a non-harmonic applied to the clock input, again the relation between analog frequency and clock rate must be considered by subtracting correction factor *k* (see equation (25)) from the SFDR value.

2.9.3 Intermodulation

For testing the third-order intercept point (IIP3) of a DUT, a two-tone signal at the analog ADC input is required. A common way to generate two-tone signals is to combine the output signals of two signal generators, working at different frequencies, by using a power combiner. However, the user should first consider the instrument settings of the automatic level control (ALC) loop. It is absolutely necessary to set the ALC state to the ALC OFF mode in order to avoid intermdodulation products generated by the level control loop of the used generators. This happens since the isolation between the outputs of the two instruments is limited by the power combiner used, and part of the signal from one instrument is therefore fed reversed into the output of the other instrument. Consequently, part of this signal is coupled to the signal generator's output detector, resulting in an amplitude modulation of the generator's output signal with the difference frequency of the generators that are used. The corresponding AM sidebands are visible in the output spectrum as shown in Fig. 11. The figures below illustrate the effect of the ALC settings for a two-tone signal generated by combining the output signal of two signal generators using a resistive power combiner.

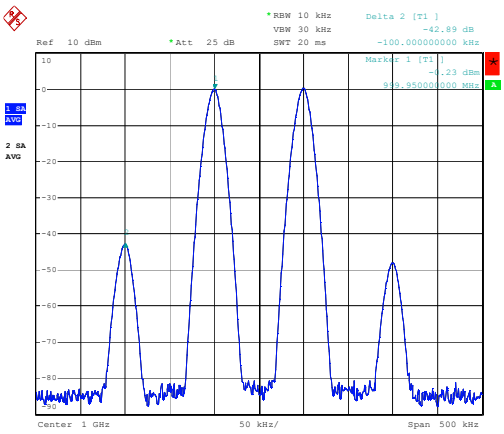

Fig. 11: Output spectrum using ALC state AUTO.

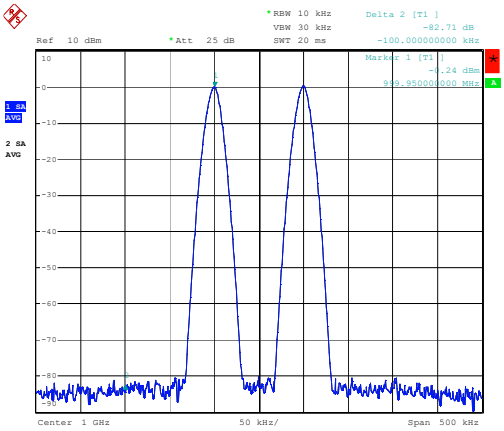

Fig. 12: Output spectrum using ALC state OFF (sample & hold).

3 Performance of the R&S®SMA100A for ADC Testing

Spectral purity is by far the most limiting factor for a potential signal source. Since spectral purity consists of noise, harmonics and non-harmonics, the selection criteria discussed in this application note focus predominantly on the generator's specifications for these parameters.
Ultimately, these factors determine a potential candidate for signal or clock source for an ADC test setup.
This section provides typical data for the spectral purity of the *R&S®SMA100A* analog signal generator with the *R&S®SMA-B22* enhanced phase noise option installed. The impact on ADC performance is described by means of examples.
The appendix provides typical performance data for the spectral purity of other analog signal generators from Rohde & Schwarz.

3.1 Phase Noise Performance

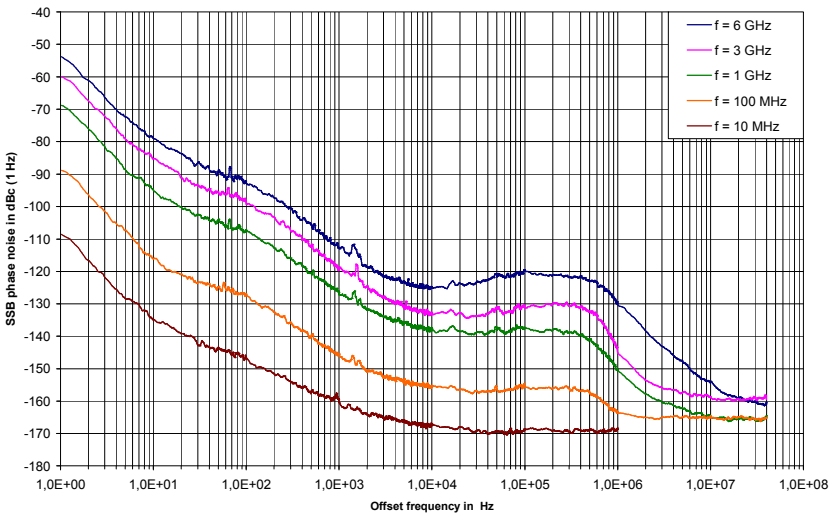

Fig. 13: R&S®SMA100A SSB phase noise.

Fig. 13 highlights the outstanding phase noise characteristic of the *R&S®SMA100A*, especially at low frequencies. Due to an innovative synthesizer concept generating low frequencies down to 6.6 MHz by dividing instead of mixing, the phase noise performance of the *R&S®SMA100A* even exceeds the performance of most standard quartzes often used as a clock source.
The phase noise performance of a signal generator is almost independent of the set output level and only the noise floor may possibly be reduced for lower output levels (see section 3.2 for details).

3.2 Wideband Noise Performance

If the wideband noise performance of a signal generator is discussed, a distinction must be made between wideband phase noise, wideband amplitude noise and overall wideband noise, which is the sum of wideband phase noise and wideband amplitude noise. For white noise, which is normally assumed for offset frequencies > 10 MHz, the amplitude- and phase-noise contribution is equal and uniformly distributed versus frequency. Therefore, the overall wideband noise is normally 3 dB higher than the wideband phase noise.
If a signal generator is utilized as the clock source, only the wideband phase noise contributes to the SNR performance of the ADC since the amplitude noise is suppressed by level-limiting differential input stages normally used in ADCs.

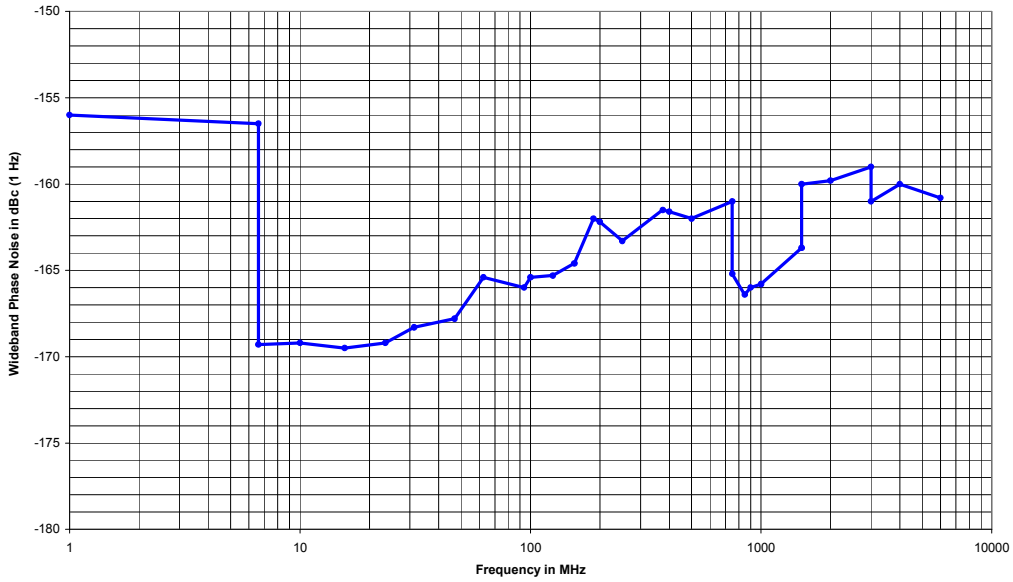

Fig. 14: R&S®SMA100A wideband phase noise performance.

Fig. 14 shows the measured wideband SSB phase noise of an R&S®SMA100A with its outstanding low phase noise performance especially at low frequencies. For frequencies below 6.6 MHz, the instrument uses a mixer to downconvert the signal, resulting in a wideband phase noise of approx. –156 dBc(Hz) in this frequency range, which is still an excellent value.

At the analog signal input of an ADC, the amplitude noise also contributes to the SNR performance. Therefore, the overall wideband noise of the analog source must be considered. Fig. 15 shows the measured overall wideband noise of an *R&S®SMA100A* vs. carrier frequency for three different output levels.

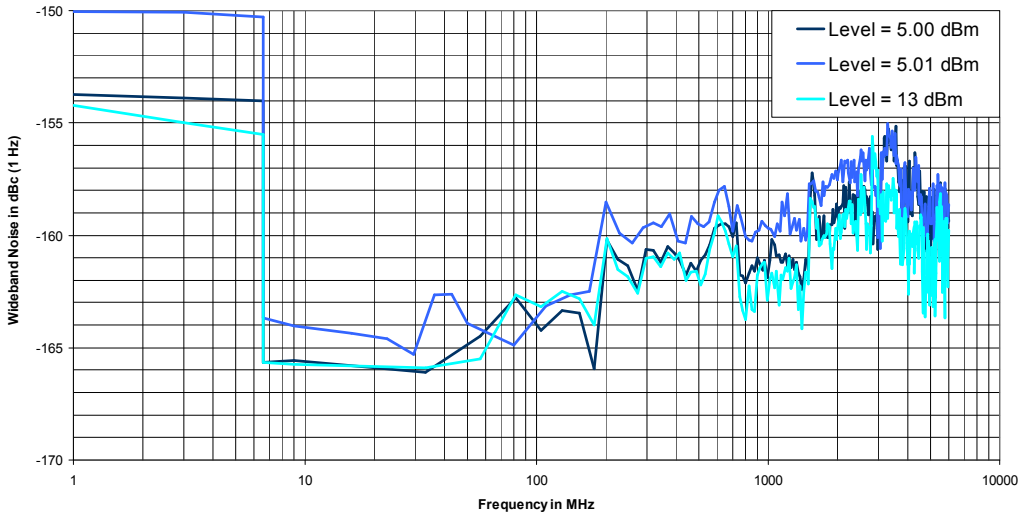

Fig. 15: R&S®SMA100A overall wideband noise vs. carrier frequency and output level.

The signal generator's wideband noise floor clearly varies somewhat versus the set output level. This is caused by the way the automatic leveling mechanism in a signal generator is implemented. Fine-level tuning is done by adjusting the gain of the RF output stage, whereas for a coarse adjustment (>5 dB), the attenuation of a discrete step attenuator, which follows the RF output stage, is changed in addition. The available dynamic range for the fine-level tuning is approx. 20 dB. However, for the best overall performance, only 5 dB are used in the AUTO attenuator mode.

Assuming that the change-over points for the discrete step attenuator are at 0 dBm and 5 dBm generator output power, the discrete step attenuator remains constant between 0.01 dBm and 5.00 dBm, and all level settings are made by adjusting the output level of the RF output stage, which reaches its maximum at 5.00 dBm. If the output level is increased from 5.00 dBm to 5.01 dBm, the attenuation of the step attenuator is decreased by 5 dB and, accordingly, the output level of the output stage must be decreased by 4.99 dB. Since the signal generator's wideband noise performance mainly depends on the signal level at the RF output stage and becomes worse if its level is decreased, the wideband noise at 5.01 dBm is worse than at 5.00 dBm even though the generator's output level has increased, as can be seen in Fig. 15.
The wideband noise performance can be optimized by increasing the level at the RF output stage, which is achieved by changing the attenuator settings mode from AUTO to FIXED. In the attenuator settings mode FIXED, the discrete step attenuator will no longer be changed.

Example: The following example for a sequence of settings shows the use of the FIXED attenuator mode at an output level of 5.01 dBm in order to optimize wideband noise performance:

- Set generator level 3 dB below wanted level (e.g. 2.01 dBm).
- Set attenuator mode to FIXED.
- Set generator level to wanted output level (e.g. 5.01 dBm).
- Check whether an ALC unlocked error is indicated on the instrument. If so, use the AUTO attenuator mode.

With these settings, the attenuation of the step attenuator is 5 dB higher than compared to the AUTO attenuator mode. Therefore, the output level of the output stage is also increased by 5 dB, which provides better wideband noise performance.

If the instrument indicates an ALC loop error, it is not possible to use these special attenuator settings. However, these settings are not necessary in this case since the output stage is already running at a high output level. This means that the wideband noise performance is already at its optimum with the AUTO attenuator mode.

But one point needs to be kept in mind when applying these settings: The harmonic performance of the signal generator will be degraded as a result of the higher output level of the output stage (see section 3.6).

3.3 Jitter and SNR Performance of the R&S®SMA100A as a Clock Source

Fig. 16 shows RMS jitter values derived from phase noise measurements indicated in Fig. 13. The jitter bandwidth for SSB phase noise integration is 10 kHz to 40 MHz for the light blue trace and 10 kHz to 10 MHz for the dark blue trace, representing a clock bandwidth of 80 MHz and 20 MHz, respectively.

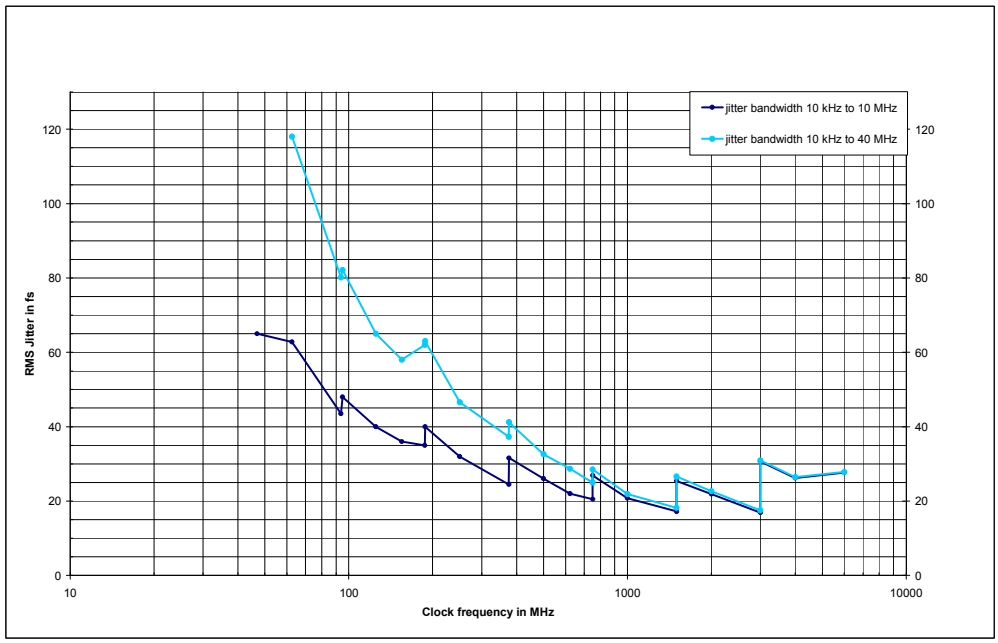

Fig. 16: RMS jitter vs. clock frequency for the R&S®SMA100A.

Fig. 16 shows that RMS jitter rises to lower frequencies, although the phase noise decreases for lower carrier frequencies as shown in Fig. 13.

If a signal is divided by an ideal frequency divider, theory tells us that the phase noise of the signal will also be divided by the same division factor and the RMS jitter of the signal will remain constant. Mathematically, equation (13) shows that the numerator and the denominator are divided by the same division factor and, therefore, the result for RMS jitter is constant.

In reality, an ideal divider is not available, which means that the wideband phase noise is limited to the divider's noise floor. If this limit is reached, the phase noise is not divided further as described above. As a consequence, the RMS jitter increases for lower frequencies. In Rohde & Schwarz signal generators, a sophisticated, ultra-low-noise divider is used to reach an extremely low noise floor of down to -170 dBc(Hz). Such performance is not accomplished from commercially available off-the-shelf dividers, generating a typical noise floor of approx. -150 dBc(Hz).

Compared to high-end instruments from the market's primary competitors, using a downconverter or commercial off-the-shelf divider for generating frequencies below 250 MHz, the jitter performance of the *R&S®SMA100A* is considerably better as shown in Fig. 17 below.

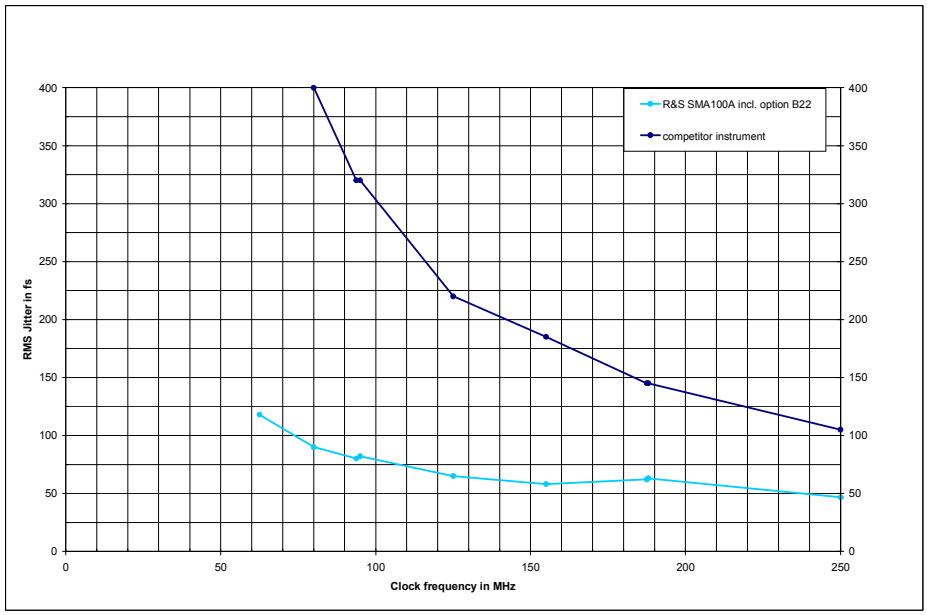

Fig. 17: Comparison of measured RMS jitter for the R&S®SMA100A and competitor instrument for jitter bandwidth = 10 kHz to 40 MHz vs. clock frequency.

The following figure shows the SNR contribution due to clock jitter derived from RMS jitter as shown in Fig. 16 using equation (10). The SNR is shown vs. clock frequency for three different analog input frequencies (10 MHz, 100 MHz and 1 GHz) and for a clock bandwidth of 20 MHz (solid trace) and 80 MHz (dotted trace).

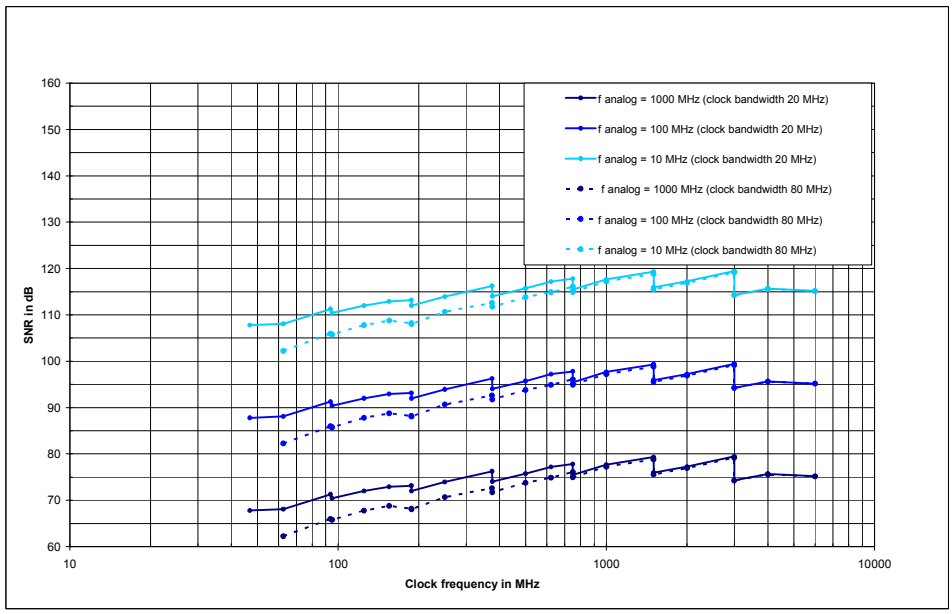

Fig. 18: SNR contribution from clock jitter vs. clock frequency and analog input frequency for the R&S®SMA100A.

In many applications, the clock bandwidth that is used is much higher than the 20 MHz or 80 MHz used for SNR calculation in Fig. 18. For such wideband applications, the wideband phase noise of the clock source must be considered for SNR calculation as shown in section 2.6. Equation (23) describes the relation between wideband phase noise, clock bandwidth, relation between clock and signal frequency and SNR. The following diagram provides SNR characteristic vs. clock bandwidth for various wideband phase noise performance levels and under the assumption that the analog signal frequency is equal to the clock rate.

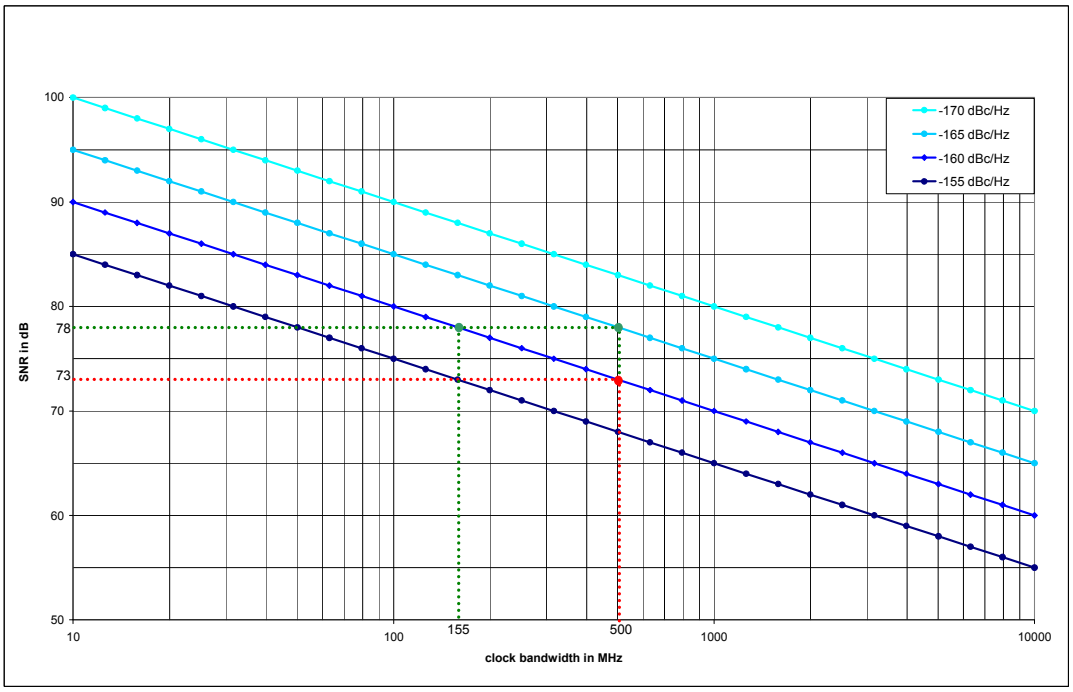

Fig. 19: SNR vs. clock bandwidth and wideband phase noise, fanalog = fclk.

Knowing the implemented clock bandwidth and the wideband phase noise performance of the implemented clock source, the SNR contribution due to clock jitter can be estimated using Fig. 19.

If the SNR for different analog input frequencies is needed, it is required to correct the values taken from Fig. 19 as follows, which is graphically shown in Fig. 9:

$$k = -20 \cdot \log\left(f_{ana\log} \Big/ f_{clk} \right) \tag{30}$$

Example: A 14-bit ADC running at a clock rate of 200 MSPS and an analog input frequency of 100 MHz is specified with a max. SNR of 73 dB (see Fig. 7). With a clock bandwidth of 500 MHz and a wideband phase noise from the clock source of –160 dBc(Hz), Fig. 19 yields an SNR value of 73 dB. Since the analog input frequency at the ADC is half the clock rate, according to equation (30), a correction value of 6 dB must be added, resulting in an SNR contribution from the clock source of 79 dB. According to equation (20) and Fig. 20 below, the total SNR performance of the ADC is reduced – as a result of the non-ideal clock source – by 1 dB to 72 dB. Improving the wideband phase noise performance of the clock source by 5 dB would reduce this SNR deterioration to 0.33 dB. The same SNR improvement could be achieved by reducing the clock bandwidth from 500 MHz to 155 MHz, as graphically depicted in Fig. 19.

The SNR deterioration due to the addition of two SNR contributors is graphically illustrated in Fig. 20.

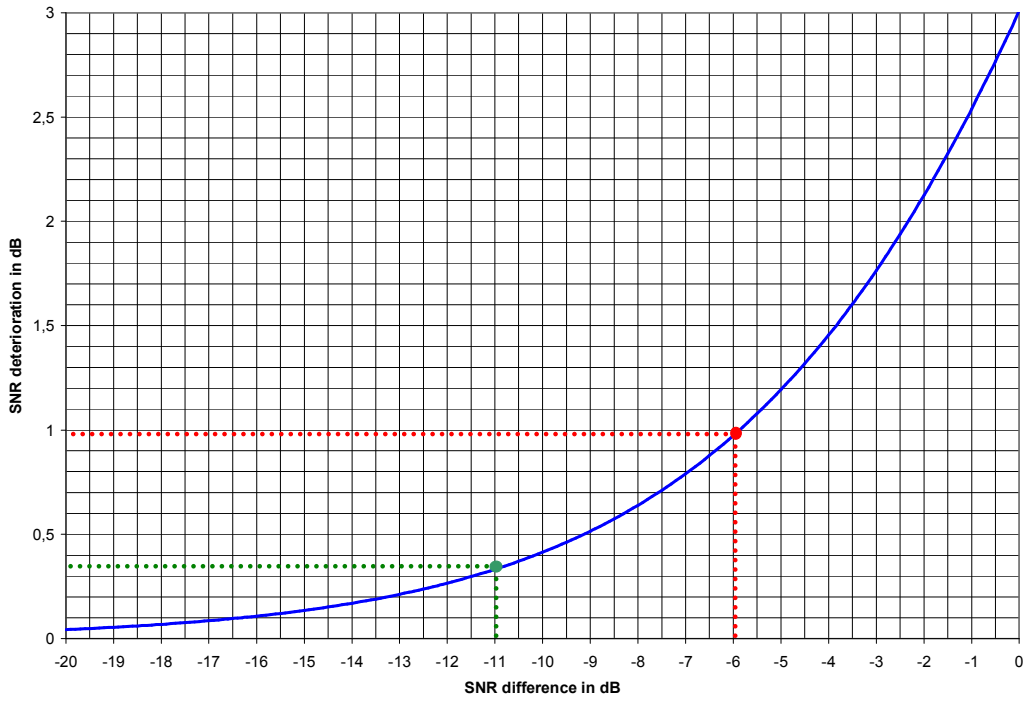

Fig. 20: SNR deterioration vs. SNR difference of two SNR contributions.

The dotted red lines show an SNR reduction of 1 dB if the difference between the two contributors is 6 dB, and the dotted green lines show an SNR impairment of 0.33 dB for a difference of 11 dB (see example above).

Fig. 21 depicts the calculated SNR contribution for the *R&S®SMA100A* as clock source vs. clock rate and three different clock bandwidths (10 MHz, 100 MHz and 1 GHz), evaluated from the wideband phase noise performance indicated in Fig. 14 by use of equation (23).

The analog input frequency is equal to the clock rate for this calculation.

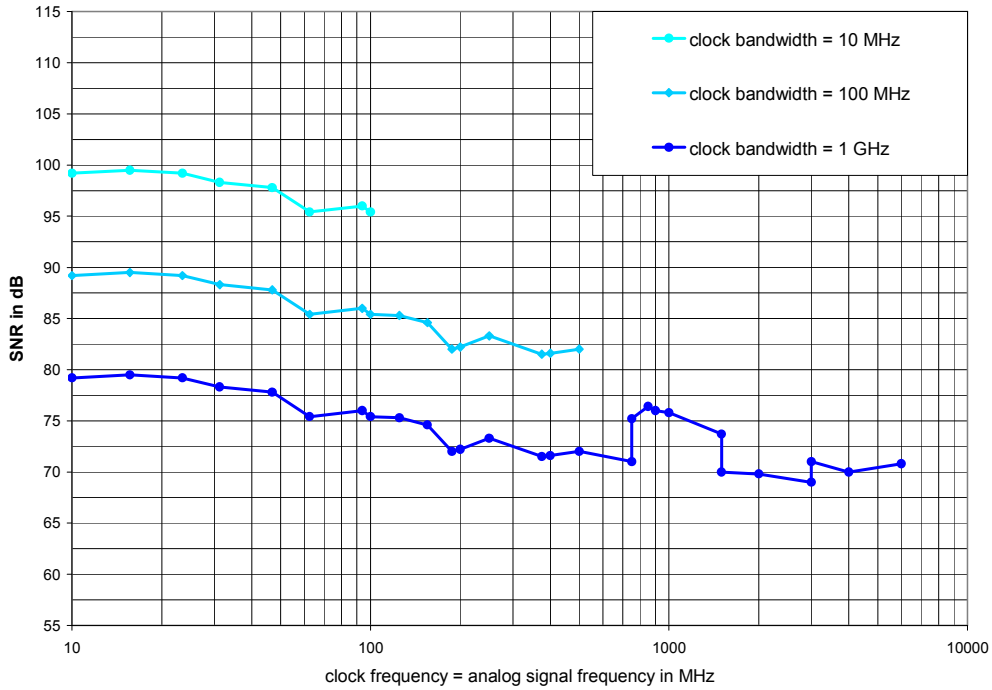

Fig. 21: SNR vs. clock rate and clock bandwidth for the R&S®SMA100A and $f_{analog} = f_{clk}$.

If the SNR for different analog input frequencies is needed, the relation between clock rate and f_{analog} must be considered by adding the correction value given from equation (30) to the SNR values from Fig. 21.
Calculating the SNR value for a different clock bandwidth is possible by correcting the SNR value from Fig. 21 using the following equation.

$$SNR_{BW2} = SNR_{BW1} - 10\log_{10}\left(\frac{BW2}{BW1}\right) \qquad (31)$$

Example: If the clock bandwidth is reduced from 1 GHz to 500 MHz, the SNR will be improved by 3 dB; Inversely, if the clock bandwidth is increased from 100 MHz to 200 MHz, the SNR will deteriorate by 3 dB.

3.4 SNR Performance for the R&S®SMA100A as Analog Source

Fig. 22 depicts the calculated SNR contribution for the *R&S®SMA100A* as analog signal source vs. analog input frequency and three different analog bandwidths (10 MHz, 100 MHz and 1 GHz), calculated from the overall wideband noise performance at 5.00 dBm indicated in Fig. 15 by using equation (24).

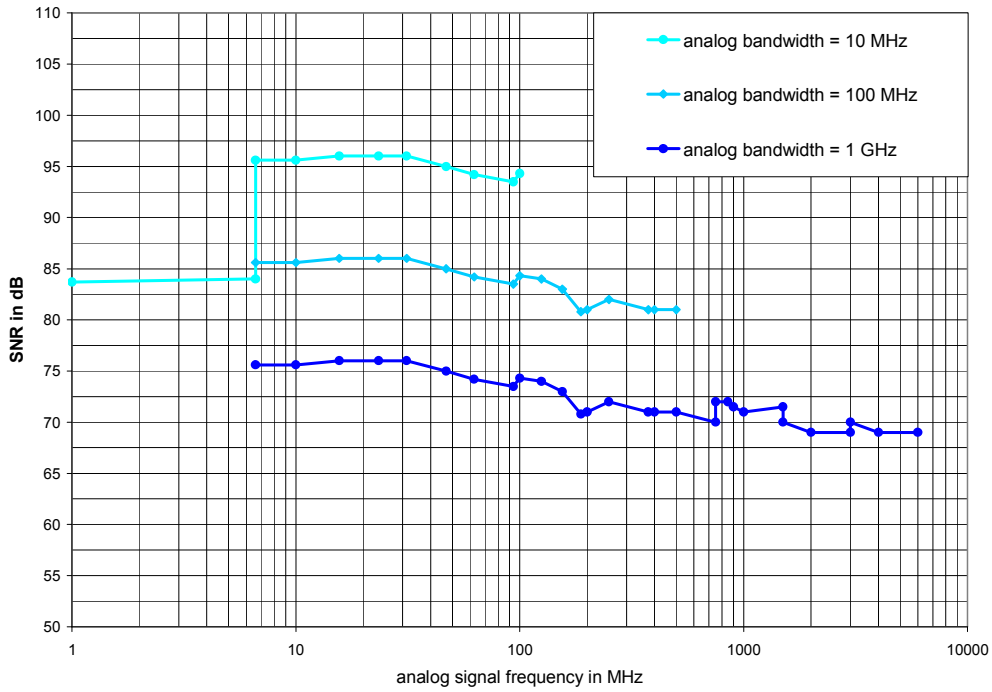

Fig. 22: SNR vs. analog signal frequency and analog bandwidth for the R&S®SMA100A.

Calculating the SNR value for a different analog bandwidth is equal to the correction for a different clock bandwidth by correcting the values from Fig. 22 by using equation (31) above.

Example: If the analog bandwidth is reduced from 1 GHz to 500 MHz, the SNR will be improved by 3 dB. Inversely, if the analog bandwidth is increased from 100 MHz to 200 MHZ, the SNR will deteriorate by 3 dB.

3.5 Non-Harmonics

3.5.1 SFDR Due to Non-Harmonics

The SFDR performance of a signal generator is normally dominated by its harmonic distortion since the level of the harmonics is much higher than the level of non-harmonic spurious.

However, by using adequate filtering at the generator's output, the harmonic signal components can be suppressed effectively and only non-harmonic spurious will then contribute to the signal generator's SFDR performance.

The SFDR contribution for a symmetrical non-harmonic spur, present at the analog signal input of an ADC, with a typical and specified spur performance of the *R&S®SMA100A* is shown in Fig. 23 below.

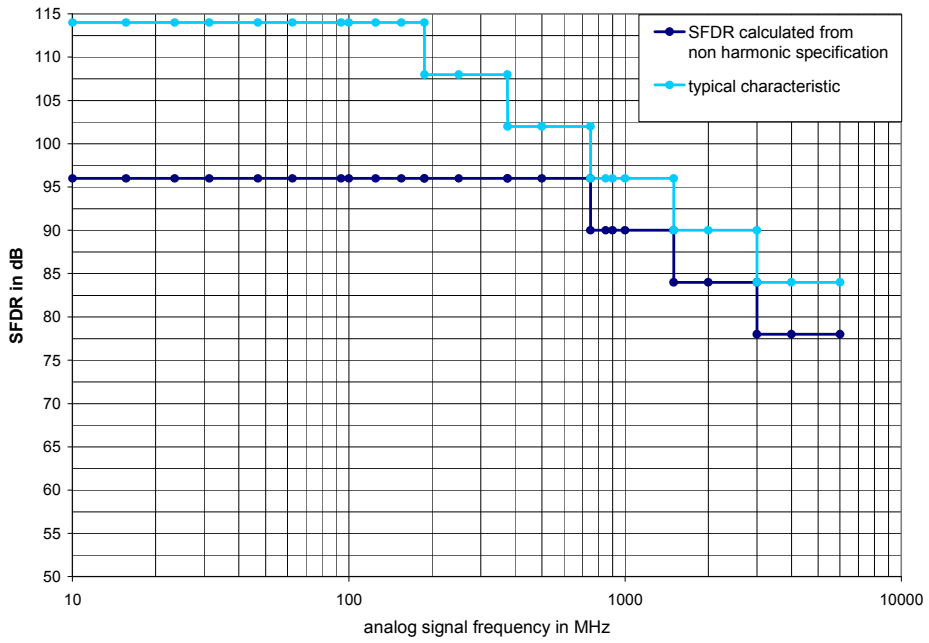

Fig. 23: SFDR performance of the R&S®SMA100A due to a non-harmonic spurious versus analog signal frequency.

The typical SFDR performance is approx. 6 dB better than the specified characteristic from Fig. 23. Plus, for frequencies less than 375 MHz, the divider concept delivers a further improvement of 6 dB for each frequency octave below 375 MHz. However, values below 96 dBc are typical values only, and are not assured by Rohde & Schwarz since it is almost impossible to verify these characteristics during production.

Fig. 23 is also valid for the clock input if the analog signal frequency is equal to the clock rate; otherwise, the SFDR must be corrected by the relation between analog signal frequency and clock rate, just like for phase noise (see equation (30)).

3.5.2 Jitter Contribution of Non-Harmonics

The following diagram shows the RMS jitter contribution due to non-harmonic spur levels. The typical RMS jitter performance of the *R&S®SMA100A,* incl. option B22 due to phase noise for 80 MHz bandwidth, is also plotted in Fig. 24 in order to estimate the spur level at which the jitter due to the spur is higher than the jitter due to phase noise. The dotted red line depicts the RMS jitter contribution of a non-harmonic spur equal to the specified performance of the *R&S®SMA100A* with option B22.

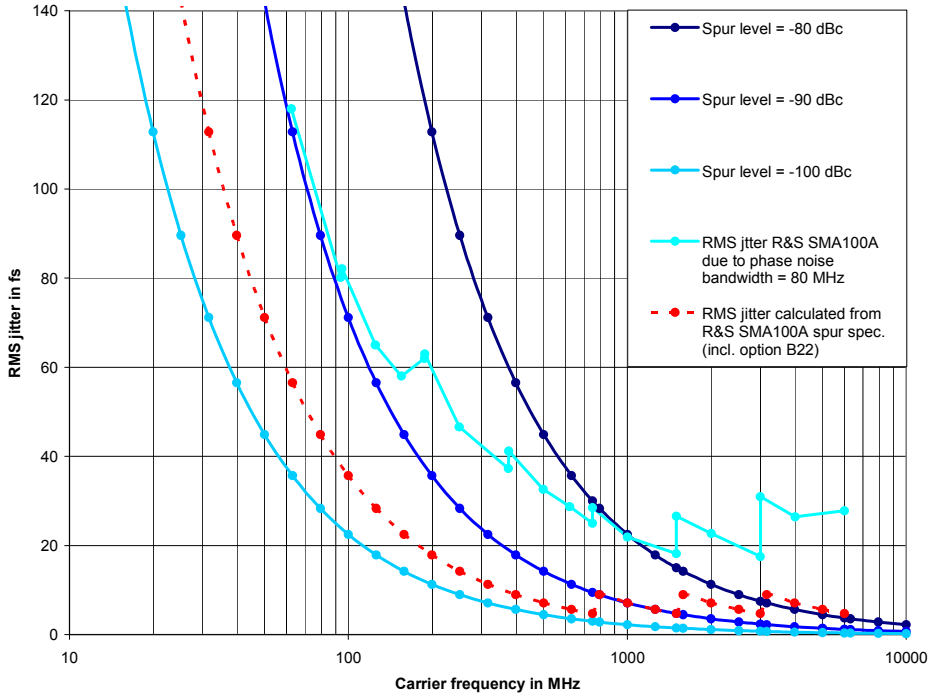

Fig. 24: RMS jitter contribution due to non-harmonic spurs and typical RMS jitter performance of the R&S®SMA100A vs. carrier frequency.

For high frequencies, Fig. 24 illustrates that a spur performance of 80 dBc to 90 dBc normally does not affect the generator's jitter performance, but for low frequencies, non-harmonic suppression of 90 dBc to 100 dBc is absolutely required.

Fig. 24 also clearly shows that the jitter performance of the *R&S®SMA100A* is dominated by phase noise performance instead of spurious performance over the complete frequency range: The trace for RMS jitter due to phase noise (light blue) is considerably higher than the dotted red trace representing the jitter due to non-harmonics.

3.5.3 SNR Contribution of Non-Harmonics

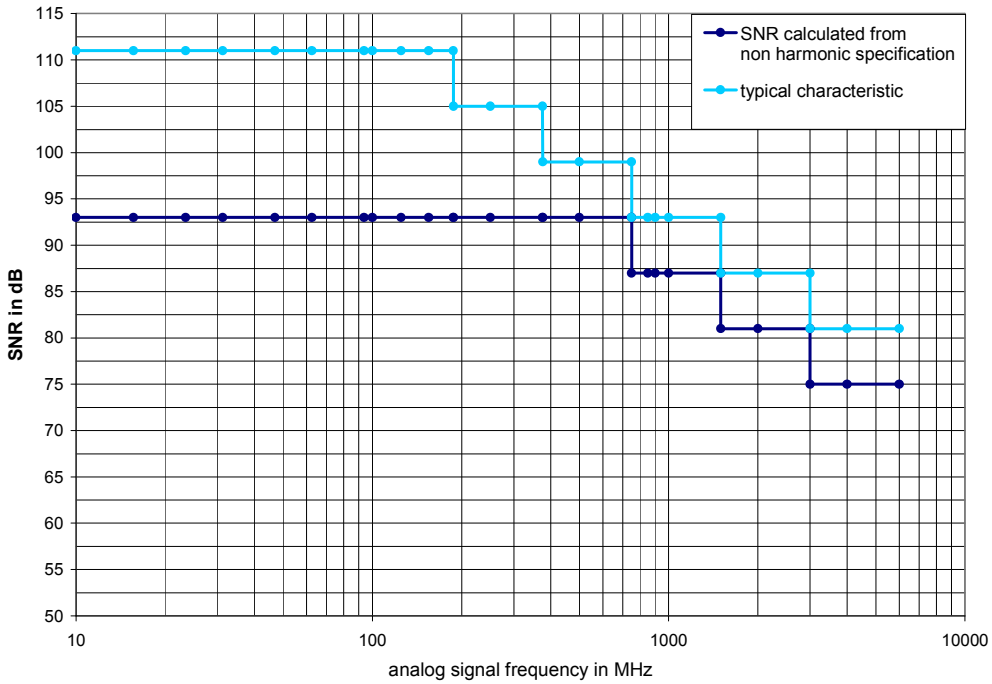

Fig. 25: SNR performance of the R&S®SMA100A due to a non-harmonic spurious vs. analog signal frequency.

Fig. 25 shows the SNR contribution for a symmetrical non-harmonic spur, equal to the spur specification of *R&S®SMA100A*, present at the analog signal input of an ADC. Fig. 25 is also valid for the clock input if the analog signal frequency is equal to the clock rate; otherwise, the SNR must be corrected by the relation between analog frequency and clock rate, just like for phase noise (see equation (30)).

The typical SNR performance is approx. 6 dB better than the values calculated from the specified non-harmonics characteristic as shown in Fig. 25. Plus, for frequencies below 375 MHz, the divider concept delivers a further improvement of 6 dB for each frequency octave below 375 MHz.

3.6 Harmonics

The typical harmonic distortion for the second and third harmonic of the *R&S®SMA100A* is depicted in Fig. 26 for an output level of +9 dBm. The harmonics with higher orders are normally far below these values.

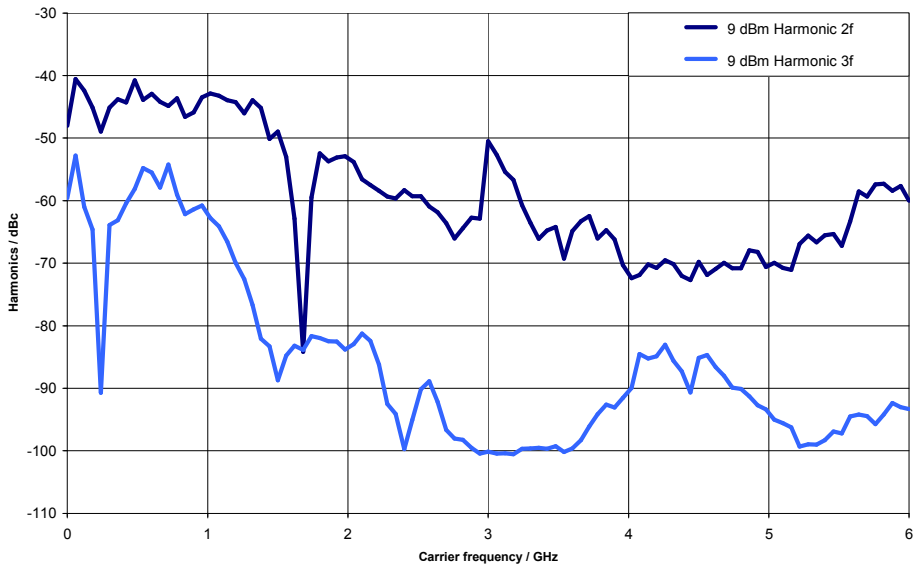

Fig. 26: Measured harmonics at +9 dBm vs. carrier frequency for the R&S®SMA100A.

The harmonic distortion of a signal generator varies versus the set output level and mainly depends on the signal level at the RF output stage. This signal level depends on the set generator level and also on the setting of the discrete step attenuator which follows the output stage. Fine level tuning is done by adjusting the gain of the RF output stage, whereas for a coarse adjustment (>5 dB), the attenuation of the discrete step attenuator is changed in addition. The available dynamic range for fine level tuning is approx. 20 dB, but for best overall performance, a figure of only 5 dB is used in the AUTO attenuator mode.

Assuming that the changeover points for the discrete step attenuator are at 5 dBm and 0 dBm generator output power, the discrete step attenuator remains constant between 5.00 dBm and 0.01 dBm and all settings of levels are performed by adjusting the output level of the RF output stage, which reaches its minimum at 0.01 dBm. If the output level is decreased from 0.01 dBm to 0.00 dBm, the attenuation of the step attenuator is increased by 5 dB and, accordingly, the output level of the output stage must be increased by 4.99 dB. Since the signal generator's harmonic performance mainly depends on the signal level at the RF output stage and since it becomes worse if its level is increased, the harmonics at 0.00 dBm are worse than at 0.01 dBm even though the generator's output level has decreased.

Harmonic performance can be optimized by decreasing the level at the RF output stage, which is achieved by changing the attenuator mode from AUTO to FIXED. In the FIXED attenuator mode, the discrete step attenuator will no longer be changed.

Example: The following example of a sequence of setting steps shows the use of the FIXED attenuator mode at an output level of 0.00 dBm in order to optimize harmonic performance:

- Set the generator level 10 dB above the wanted level (e.g. 10.00 dBm).
- Set the attenuator settings to FIXED.
- Set the generator level to the wanted output level (e.g. 0.00 dBm).

With these settings, the attenuation of the step attenuator is 10 dB lower than with the AUTO attenuator mode and, therefore, the output level of the output stage is also decreased by 10 dB. Consequently, the figure for the second harmonic is as much as 10 dB lower, and the figure for the third harmonic level is as much as 20 dB lower.

It is also possible to activate the FIXED attenuator mode at a level that is 15 dB or 20 dB higher than for the wanted generator level in order to achieve even lower harmonics. However, the level accuracy is reduced in this case. With these settings, also keep in mind that the wideband noise performance of the signal generator will be degraded as a result of the lower output level present at the output stage (see section 3.2).

4 Example SNR Calculations for a Typical ADC Test Setup

This chapter provides some example SNR calculations for the *R&S®SMA100A* as a clock and analog source using the characteristics shown in chapter 3.

4.1 Typical ADC Test Setup

Fig. 27 depicts a typical setup for ADC performance testing. In general four instruments are required: a *source signal generator,* a *sample clock generator*, a *power supply* and a PC with the necessary FFT software. For most AD converters, an evaluation board with a PC interface, e.g. USB, and the required software tools are available. Most ADC evaluation boards include some level shifters or signal transformers in order to convert a sine wave signal at the board input to the required signal for the analog or clock input of the DUT, e.g. a differential signal for analog input.

The source signal generator and the sampling clock generator should be synchronized using the 10 MHz reference frequency. Therefore, the phase noise or jitter of both signal generators is correlated within the signal generator's reference PLL bandwidth and does not contribute to the test result. The reference PLL bandwidth depends on the signal generator that is used and is normally in the range of a few Hz up to 100 Hz.

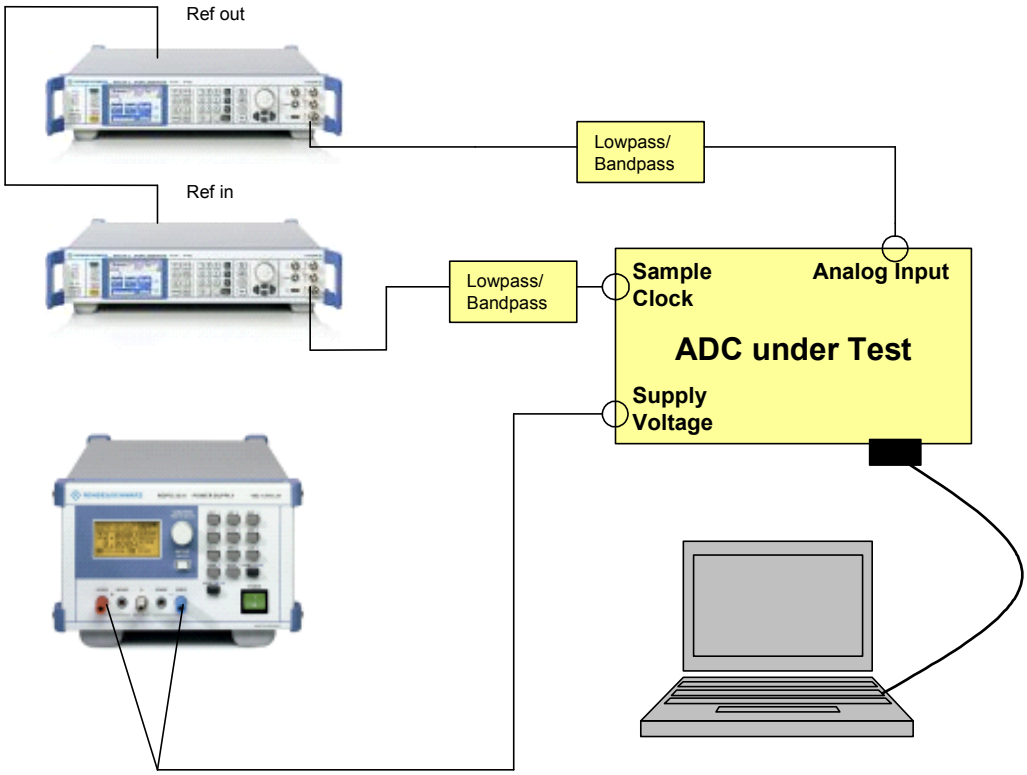

Fig. 27: General ADC performance test setup.

The two most import instruments in the above setup are the *source signal generator* and the *sample clock generator.* Signal and function generators are available with a wide variety of specifications and in a wide price range, thus presenting the following questions:

- How can the minimum specifications of the generator be determined? In other words, which generator is “just good enough” to do the job?

- Do the source signal generator and sample clock generator need to be of the same grade?

When sourcing for a *signal generator*, the following factors must be taken into account:

- The generator’s contribution to the *wideband noise* and *close-in noise* should be negligible, or it should at least have a minimum effect on the *S/N* measurement procedure of the ADC.

- The generator’s non-harmonic distortion products should be far below the distortion products of the ADC.

- Since the demands placed on a signal source may become higher in future challenges, the performance of a purchased generator should optionally already have enough margin to meet these future requirements.

4.2 ADC Test Setup with the R&S®SMA-B29 Clock Synthesizer

The R&S®SMA100A is the only analog high-performance signal generator available on the market that combines both a clock signal source and an analog signal source in a single box. Using this option, the test setup from Fig. 27 simplifies to the setup shown below.

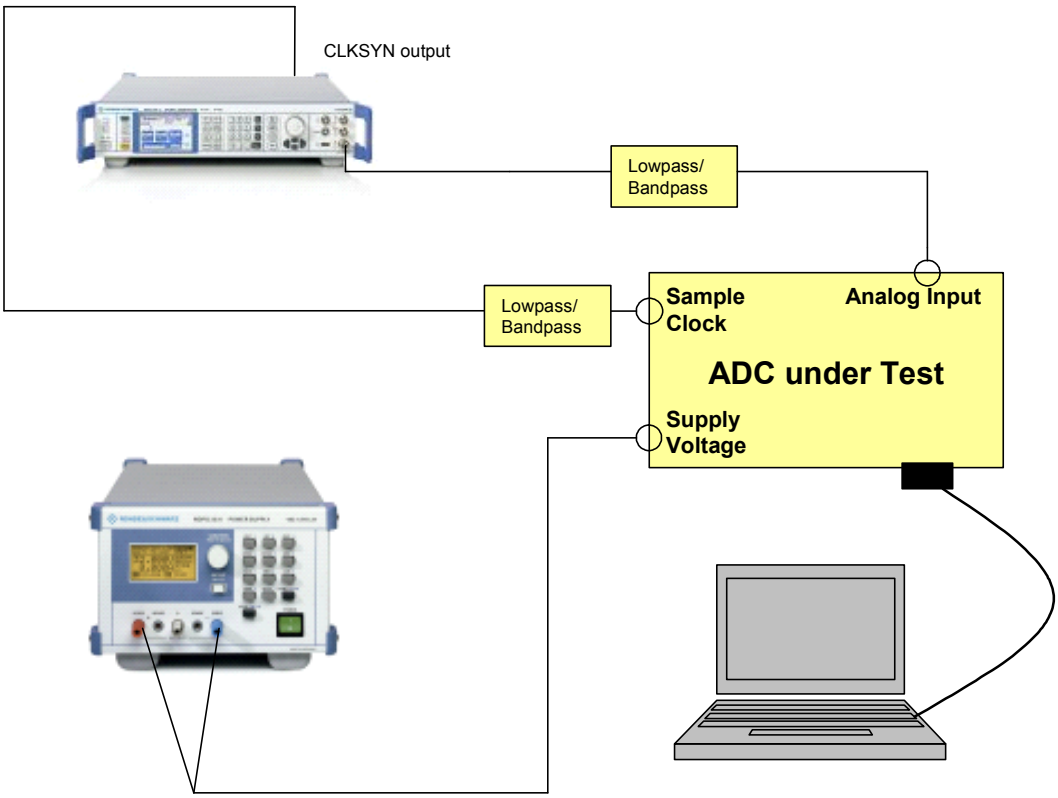

Fig. 28: Simplified ADC test setup using the R&S®SMA-B29 clock synthesizer as clock source.

If required, the clock synthesizer provides a differential output signal, thus eliminating. the need for a single-ended-to-differential signal transformer at the ADC clock input.

Since the spectral purity of the clock synthesizer is not as high as for the RF output of the R&S®SMA100A, this setup is the perfect solution for many low- and medium-performance ADCs or for applications where the clock frequency is much higher than the signal frequency.
For high-performance or undersampled applications, the performance of this setup must be verified and it may not be sufficient for some tasks. If so, the setup shown in Fig. 27 is the preferred solution to meet the higher requirements.

4.3 Typical ADC Specifications

The table below lists some typical characteristics of discrete high-speed ADCs.

ADC type	Resolution bits	Sample rate (megasamples per second)	Signal-to-noise ratio dBFS	Spurious-free dynamic range dBc
Linear Technology LTC2217	16	105	81	100
Analog Devices AD9445-125	14	125	74.1 @ 10 MHz 70 @ 450 MHz	95 @ 10 MHz 69 @ 450 MHz
National Semiconductor ADC12C080	12	80	71.2	90
Texas Instruments ADS5237	10	65	61.7	86
Maxim MAX108	8	1500	47.4	61.6

Table 2: Typical ADC characteristics.

4.4 SNR Calculation for the R&S®SMA100A

4.4.1 Setup 1: 16-bit ADC with 100 MSPS and 10 MHz Test Signal

In this example, two *R&S®SMA100A generators* are used as a clock source and analog source for a 16-bit 100 MSPS ADC test set, applying a 10 MHz sine signal at the analog input. According to Table 2, the typical SNR performance of such an ADC (LTC2217) is approx. 81 dB. Therefore, the SNR of the test setup should be far below this value.
The frequencies and bandwidths for the clock signal and the analog signal used for the calculation are listed in the following table.

Clock input		Analog input	
Frequency in MHz	**Bandwidth in MHz**	**Frequency in MHz**	**Bandwidth in MHz**
100	300	10	25

Table 3: Parameters for clock input and analog input of the ADC.

Step 1: Calculation of SNR due to jitter/phase noise of clock source
Fig. 21 shows the SNR performance of the R&S®SMA100A used as a clock source to an ADC test set. For a clock rate of 100 MHz, an analog signal frequency of 100 MHz and a clock bandwidth of 100 MHz, an SNR value of 85.5 dB can be read from the diagram.
First, the lower analog input frequency of 10 MHz must be considered and the SNR value must be corrected by using equation (30).

$$SNR_{clk\_10MHz} = SNR_{clk\_100MHz} - 20\log_{10}\left(\frac{10\,MHz}{100\,MHz}\right) = 85.5\,dB + 20\,dB = 105.5\,dB$$

Next, the SNR must be corrected due to the higher clock bandwidth of 300 MHz by using equation (31).

$$SNR_{clk\_BW300MHz} = SNR_{clk\_BW100MHz} - 10\log_{10}\left(\frac{300\,MHz}{100\,MHz}\right) = 105.5\,dB - 4.8\,dB = 100.7\,dB$$

Step 2: Calculation of SNR due to non-harmonics of clock source
It is assumed that the clock signal includes one symmetrical non-harmonic with the minimum specified suppression of 96 dBc (see Fig. 23). Fig. 25 indicates an SNR of 93 dB for such a non-harmonic. Since the clock input of the ADC is taken into account, the SNR value must be corrected by the relation between the analog frequency and the clock rate according to equation (30).

$$SNR_{spur\_clk\_100MHz} = SNR_{spur\_ana\log\_100MHz} - 20\log_{10}\left(\frac{10\,MHz}{100\,MHz}\right) = 93\,dB + 20\,dB = 113\,dB$$

Step 3: Calculation of SNR due to jitter/phase noise of analog source
Fig. 22 shows the SNR performance of the *R&S®SMA100A* used as the analog source to an ADC test set. For an analog signal frequency of 10 MHz and an analog bandwidth of 100 MHz, an SNR value of 86 dB can be read from the diagram.
Since the analog input bandwidth is only 25 MHz in this example, the SNR must be corrected by equation (31).

$$SNR_{ana\log\_BW25MHz} = SNR_{ana\log\_BW100MHz} - 10\log_{10}\left(\frac{25\,MHz}{100\,MHz}\right) = 86\,dB + 6\,dB = 92\,dB$$

Step 4: Calculation of SNR due to non-harmonics of analog source
It is assumed that the analog signal includes one symmetrical non-harmonic with a typical suppression of 114 dBc. Fig. 25 indicates an SNR of 111 dB for such a non-harmonic.

$$SNR_{spur\_ana\log\_10MHz} = 111\,dB$$

Step 5: Summary
All SNR contributors must be added together to determine the SNR limitation of the test set that is used (without DUT).

$$SNR_{test\_set} =$$

$$-10\log_{10}\left(10^{-SNR_{clk\_BW300MHz}/10} + 10^{-SNR_{spur\_clk\_100MHz}/10} + 10^{-SNR_{ana\log\_BW25MHz}/10} + 10^{-SNR_{spur\_ana\log\_10MHz}/10}\right)$$

$$SNR_{test\_set} = 91.2\,dBc$$

This SNR estimation shows that a test set using two R&S®SMA100A generators as the clock source and the analog source has a margin of approx. 10 dB from the typical 16-bit ADC indicated in Table 2.

Fig. 20 shows that the SNR deterioration due to the limited performance of the test set that is used is approx. 0.4 dB in this example.
The most effective way to improve the performance of the test set in this example is to reduce the bandwidth of the analog source by using lowpass or bandpass filters. The achievable SNR performance of the test set and the corresponding SNR deterioration for a DUT with SNR = 81 dB are shown in the following table.

Bandwidth analog source in MHz	25	10	5	2.5
SNR of test set in dB	91.2	94.6	96.5	97.9
SNR deterioration of measured DUT (SNR = 81 dB)	0.4	0.2	0.14	0.09

Table 4: SNR improvement due to reduced analog bandwidth.

If the contribution of the test set to the measured SNR must be below 0.1 dB, a 2.5 MHz bandpass filter must be used at the analog input of the DUT.
The SFDR performance of typ. 100 dBc of this DUT can be tested only if the harmonic signal components of the signal generator (see Fig. 26) are suppressed by approx. 70 dB by using adequate filters at the analog input.
The typical non-harmonic performance of the *R&S®SMA100A* is sufficient for this test.

4.4.2 Setup 2: R&S®SMA-B29 Used as Clock Source in Setup 1

In this example, setup 1 is modified by replacing the *R&S®SMA100A* being used as a clock source with the R&S®SMA-B29 clock synthesizer option installed on the *R&S®SMA100A* that is being used as the analog signal source (see setup shown in Fig. 28).
To compare the performance of the two setups, the frequencies and bandwidth used for the calculation are identical to example 1 (see Table 3).

Step 1: Calculation of SNR due to jitter/phase noise of clock source
Fig. 46 shows the SNR performance of the *R&S®SMA-B29* used as the clock source to an ADC test set. For a clock rate of 100 MHz, an analog signal frequency of 100 MHz and a clock bandwidth of 100 MHz, an SNR value of 81 dB can be read from the diagram.
First, the lower analog input frequency of 10 MHz must be considered and the SNR value must be corrected by using equation (30).

$$SNR_{clk\_10MHz} = SNR_{clk\_100MHz} - 20\log_{10}\left(\frac{10\,MHz}{100\,MHz}\right) = 81\,dB + 20\,dB = 101\,dB$$

Next, the SNR must be corrected due to the higher clock bandwidth of 300 MHz by using equation (31).

$$SNR_{clk\_BW300MHz} = SNR_{clk\_BW100MHz} - 10\log_{10}\left(\frac{300\,MHz}{100\,MHz}\right) = 101\,dB - 4.8\,dB = 96.2\,dB$$

Step 2: Calculation of SNR due to non-harmonics of clock source
It is assumed that the clock signal includes one symmetric non-harmonic with the minimum specified suppression. Fig. 25 indicates an SNR of 78 dB for such a non-harmonic. Since the clock input of the ADC is taken into account, the SNR value must be corrected by the relation between analog frequency and clock rate according to equation (30):

$$SNR_{spur\_clk\_100MHz} = SNR_{spur\_ana\log\_100MHz} - 20\log_{10}\left(\frac{10\,MHz}{100\,MHz}\right) = 78\,dB + 20\,dB = 98\,dB$$

Step 3: Calculation of SNR due to jitter/phase noise of analog source
See setup 1 (analog source is identical):

$$SNR_{ana\log\_BW25MHz} = 92\,dB$$

Step 4: Calculation of SNR due to non-harmonics of analog source
See setup 1 (analog source is identical):

$$SNR_{spur\_ana\log\_10MHz} = 111\,dB$$

Step 5: Summary
All SNR contributors must be added together to determine the SNR limitation of the test set (without DUT).

$$SNR_{test\_set} = 89.8\,dB$$

The calculation shows that the performance of this simplified setup is 1.6 dB worse compared to the setup using two *R&S®SMA100A* generators, but might be sufficient for many medium-performance applications.

The following table provides an SNR comparison for both setups with different analog bandwidths.

Bandwidth analog source in MHz	25	10	5	2.5
SNR in dB Setup using R&S®SMA100A RF output as clock source	91.4	94.6	96.5	97.9
SNR in dB Setup using R&S®SMA-B29 as clock source	89.8	91.8	92.7	93.3

Table 5: SNR comparison for different clock sources.

The SNR improvement that is achieved by reducing the analog bandwidth is not as high for the simplified setup using option R&S®SMA-B29 as the clock source as it is for the setup using the RF output of the R&S®SMA100A.

4.4.3 Setup 3: 14-Bit ADC with 125 MSPS and 450 MHz Test Signal

In this example, the *R&S®SMA100A* is used as the clock source and analog source for an undersampled 14-bit 125 MSPS ADC test set, using a 450 MHz sine signal at the analog input. According to Table 2, the typical SNR performance of a 14-bit ADC (AD9445-125) is approx. 77.3 dB at 10 MHz analog input frequency, and it drops to 70 dB at 450 MHz.
The following SNR calculations are accomplished for very high clock- and analog bandwidths as well as for narrow bandwidths using bandpass filters.
The frequencies and bandwidths used for the calculation are listed in Table 6.

Clock Input		Analog Input	
Frequency in MHz	**Bandwidth in MHz**	**Frequency in MHz**	**Bandwidth in MHz**
125	300	450	500
125	20 (bandpass filter)	450	50 (bandpass filter)

Table 6: Parameters of SNR due to jitter/phase noise of clock source.

Step 1: Calculation of SNR due to jitter/phase noise of clock source
Fig. 21 shows the SNR performance of the *R&S®SMA100A* used as the clock source for an ADC test set. For a clock rate of 125 MHz, an analog signal frequency of 100 MHz and a clock bandwidth of 100 MHz, an SNR value of 85.5 dB can be read from the diagram.
First, the higher analog input frequency of 450 MHz must be considered by correcting the SNR value by applying equation (30).

$$SNR_{clk\_450MHz} = SNR_{clk\_125MHz} - 20\log_{10}\left(\frac{450\,MHz}{125\,MHz}\right) = 85.5\,dB - 11\,dB = 74.5\,dB$$

Next, the SNR must be corrected due to clock bandwidth being used by applying equation (31).
For a clock bandwidth of 300 MHz, the SNR can be calculated as:

$$SNR_{clk\_BW300MHz} = SNR_{clk\_BW100MHz} - 10\log_{10}\left(\frac{300\,MHz}{100\,MHz}\right) = 74.5\,dB - 4.8\,dB = 69.7\,dB$$

Clearly, the high undersampling factor of this setup makes it impossible to obtain enough margin to test the DUT's SNR performance of approx.70 dB using a clock bandwidth of 300 MHz.
Reducing the clock bandwidth by using a 20 MHz bandpass filter improves the test set performance considerably.

$$SNR_{clk\_BW20MHz} = SNR_{clk\_BW100MHz} - 10\log_{10}\left(\frac{20\,MHz}{100\,MHz}\right) = 74.5\,dB + 7\,dB = 81.5\,dB$$

Step 2: Calculation of SNR due to non-harmonics of clock source
It is assumed that the clock signal includes one symmetrical non-harmonic with the typical suppression of 114 dBc (see Fig. 23). Fig. 25 provides an SNR of 111 dB for such a non-harmonic. Since the clock input of the ADC is taken into consideration, the SNR value must be corrected by the relation between analog frequency and clock rate according to equation (30).

$$SNR_{spur\_clk\_125MHz} = SNR_{spur\_ana\log\_125MHz} - 20\log_{10}\left(\frac{450\,MHz}{125\,MHz}\right) = 111\,dB - 11\,dB = 100\,dB$$

Step 3: Calculation of SNR due to jitter/phase noise of analog source
Fig. 22 shows the SNR performance of an *R&S®SMA100A* used as the analog source for an ADC test set. For an analog signal frequency of 450 MHz and an analog bandwidth of 100 MHz, an SNR value of 81 dB can be read from the diagram.
Since the analog input bandwidth is 500 MHz or 50 MHz respectively, the SNR must be corrected by using equation (31).

$$SNR_{ana\log\_BW500MHz} = SNR_{ana\log\_BW100MHz} - 10\log_{10}\left(\frac{500\,MHz}{100\,MHz}\right) = 81\,dB - 7\,dB = 74\,dB$$

$$SNR_{ana\log\_BW50MHz} = SNR_{ana\log\_BW100MHz} - 10\log_{10}\left(\frac{50\,MHz}{100\,MHz}\right) = 81\,dB + 3\,dB = 84\,dB$$

Step 4: Calculation of SNR due to non-harmonics of analog source
It is assumed that the analog signal includes one symmetrical non-harmonic with a typical suppression of 102 dBc. Fig. 25 provides an SNR of 99 dB for such a non-harmonic.

$$SNR_{spur\_ana\log\_450MHz} = 99\,dB$$

Step 5: Summary
All SNR contributors must be added together to determine the SNR limitation of the test set that is used (without DUT).
The SNR for the high bandwidth test set can be calculated as

$$SNR_{test\_set} = 68.3\,dB$$

The performance is 2 dB worse than the typical performance of the DUT, making it insufficient for device testing.

The SNR for the test set using bandpass filters is improved to

$$SNR_{test\_set\_filter} = 79.5\,dB$$

This test set has a margin of approx. 10 dB from the typical DUT performance. Fig. 20 shows that the resulting SNR deterioration due to the limited performance of the test set that is used is 0.5 dB for this example.

The DUT's SFDR performance of 69 dBc can only be tested if the harmonic signal components of the signal generator (see Fig. 26) are suppressed by approx. 40 dB by using adequate filters at the analog input.
The typical non-harmonic performance of the *R&S®SMA100A* is sufficient for this test.

4.4.4 Setup 4: R&S®SMA-B29 Used as Clock Source in Setup 3

In the following calculation, the clock source of setup 3 is replaced by the *R&S®SMA-B29* clock synthesizer option. The calculation is only performed for the narrowband setup using a 20 MHz bandpass filter at the clock input and a 50 MHz bandpass filter at the analog input.

Step 1: Calculation of SNR due to jitter/phase noise of clock source
Fig. 46 shows the SNR performance of the *R&S®SMA-B29* option used as the clock source for an ADC test set. For a clock rate of 125 MHz, an analog signal frequency of 100 MHz and a clock bandwidth of 100 MHz, an SNR value of 82 dB can be read from the diagram.
The higher analog input frequency of 450 MHz must be considered by correcting the SNR value by means of equation (30).

$$SNR_{clk\_450MHz} = SNR_{clk\_125MHz} - 20\log_{10}\left(\frac{450\,MHz}{125\,MHz}\right) = 82\,dB - 11\,dB = 71\,dB$$

Next, the SNR must be corrected due to the clock bandwidth that is implemented by using equation (31).
For a clock bandwidth of 20 MHz, the SNR can be calculated as:

$$SNR_{clk\_BW20MHz} = SNR_{clk\_BW100MHz} - 10\log_{10}\left(\frac{20\,MHz}{100\,MHz}\right) = 71\,dB + 7\,dB = 78\,dB$$

Step 2: Calculation of SNR due to non-harmonics of clock source
It is assumed that the clock signal includes one symmetrical non-harmonic with the minimum specified suppression. Fig. 47 provides an SNR of 78 dB for such a non-harmonic. Since the clock input of the ADC is taken into consideration, the SNR value must be corrected by the relation between analog frequency and clock rate according to equation (30).

$$SNR_{spur\_clk\_125MHz} = SNR_{spur\_ana\log\_125MHz} - 20\log_{10}\left(\frac{450\,MHz}{125\,MHz}\right) = 78\,dB - 11\,dB = 67\,dB$$

Step 3: Calculation of SNR due to jitter/phase noise of analog source
See setup 3 (analog source is identical):

$$SNR_{ana\log\_BW50MHz} = 84\,dB$$

Step 4: Calculation of SNR due to non-harmonics of analog source
See setup 3 (analog source is identical):

$$SNR_{spur\_ana\log\_450MHz} = 99\,dB$$

Step 5: Summary
All SNR contributors must be added together to determine the SNR limitation of the test set that is used (without DUT).

$$SNR_{test\_set\_filter} = 66.6\,dB$$

The SNR of the test set is approx. 3.5 dB below the performance of the ADC, making it insufficient for this application.

Clearly, the performance of the *R&S®SMA-B29* clock synthesizer option is sufficient for many medium- and low- performance applications, but is not adequate for high-performance test sets – especially in undersampled applications.

5 Summary

Although recent developments in high-speed/high-resolution ADC design make it clear that the generator(s) used in a performance test setup must be high-end models such as the *R&S®SMA100A*, a medium-performance generator such as the *R&S®SMB100A* or *R&S®SMC100A* is sufficient for many ADCs.
Using a generator with unnecessarily high specifications not only consumes a large portion of the budget – it can also increase project lead time when a new instrument needs to be acquired. On the other hand, a generator with inadequate specifications can significantly under-assess the performance of the ADC.
Furthermore, the generator to be purchased should already have enough extra performance capability to meet the higher requirements of tomorrow.
The practical examples presented in this application note can help you avoid the pitfalls encountered when selecting a new generator. Rohde & Schwarz's wide range of analog signal generators include the right solution for virtually any ADC test application.

6 Appendix

6.1 Performance Data for the R&S®SMA100A

Some characteristics of the *R&S®SMA100A* can be enhanced by installing the *R&S®SMA-B22* option for achieving higher phase noise performance. If there is a difference in the characteristic, both measurements are shown below, whereas only one measurement plot is provided if there is no difference in performance.

6.1.1 SSB Phase Noise

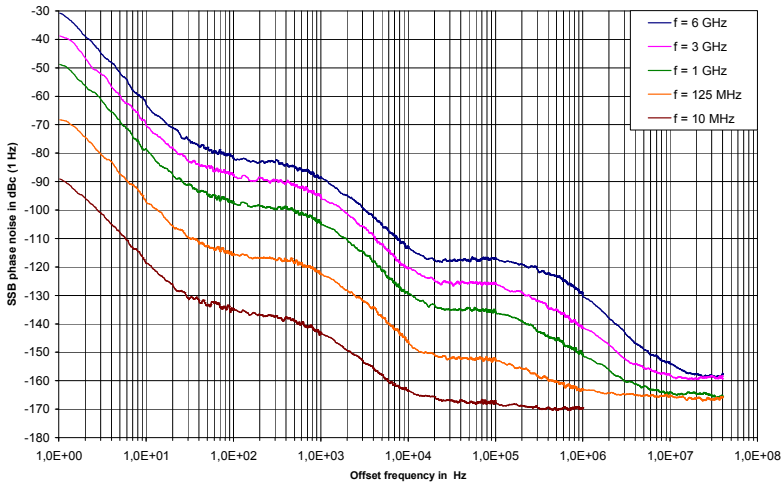

Fig. 29: R&S®SMA100A SSB phase noise (standard instrument).

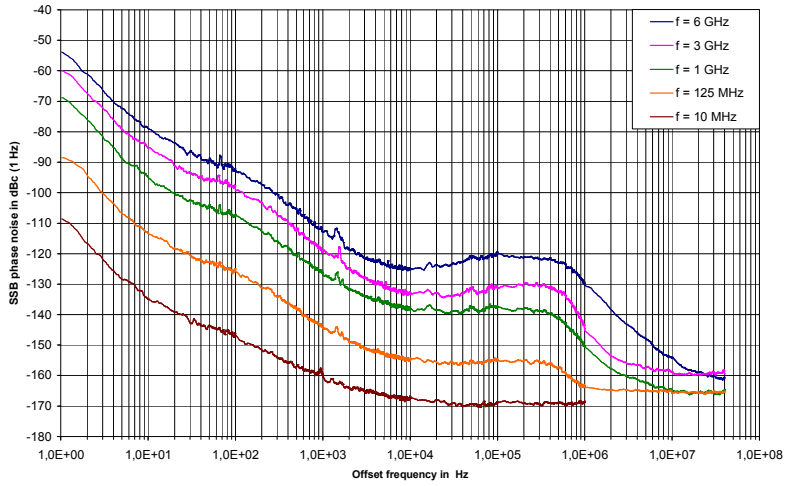

Fig. 30: R&S®SMA100A SSB phase noise with the R&S®SMA-B22 option for enhanced phase noise performance.

6.1.2 Wideband SSB Phase Noise

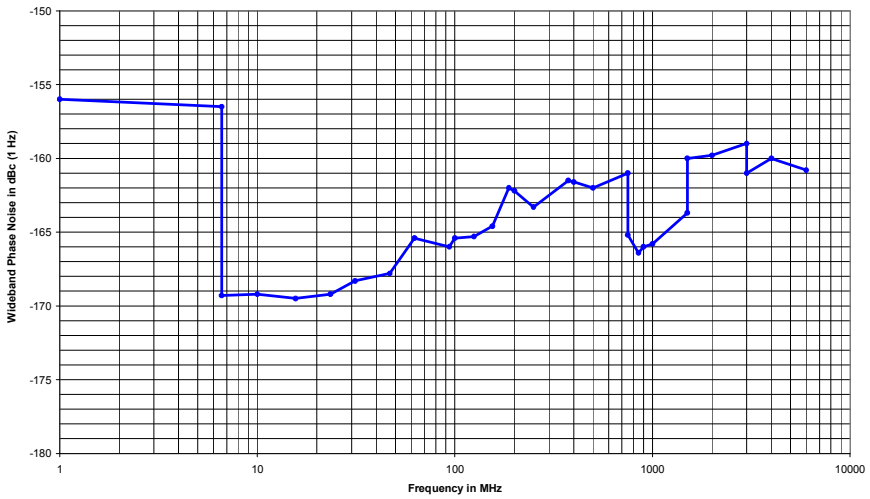

Fig. 31: R&S®SMA100A wideband phase noise performance.

6.1.3 Wideband Noise

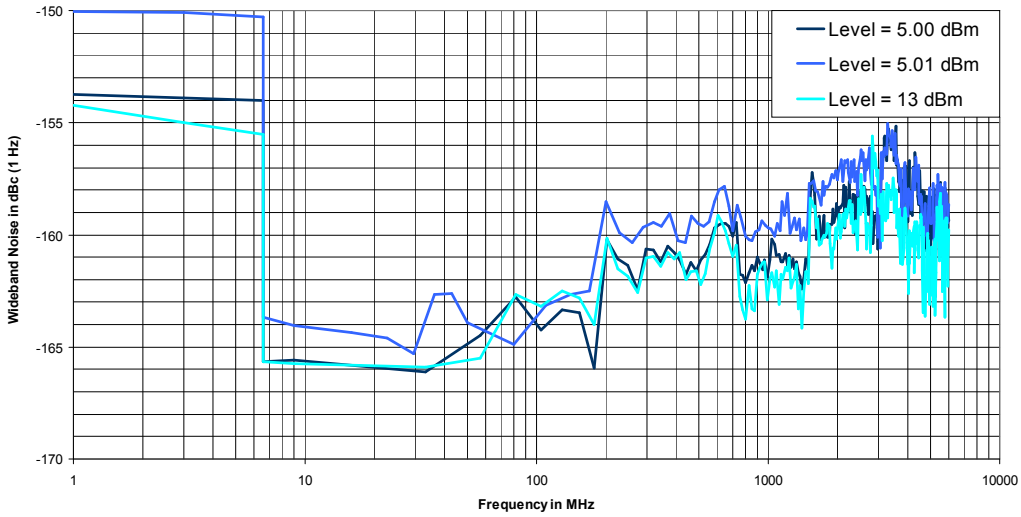

Fig. 32: R&S®SMA100A overall wideband noise vs. carrier frequency and output level.

6.1.4 RMS Jitter (Bandwidth 10 kHz to 10 MHz and 10 kHz to 40 MHz)

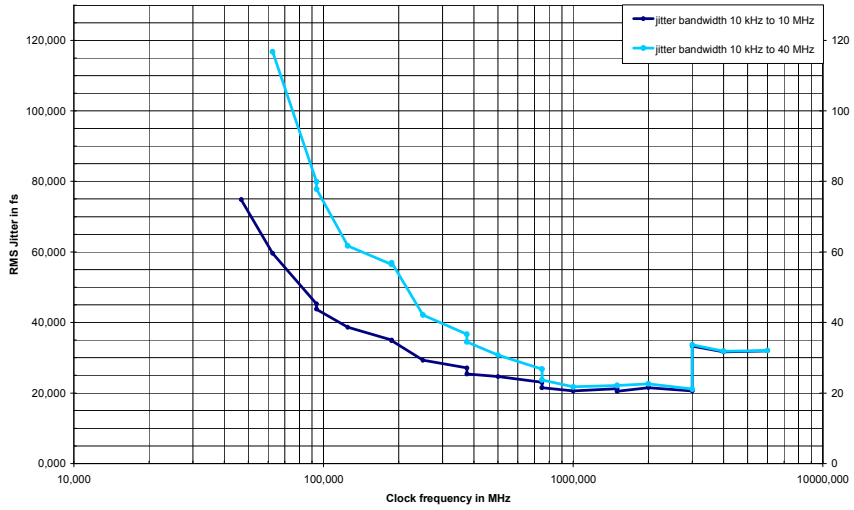

Fig. 33: RMS jitter vs. clock frequency for the R&S®SMA100A (standard instrument).

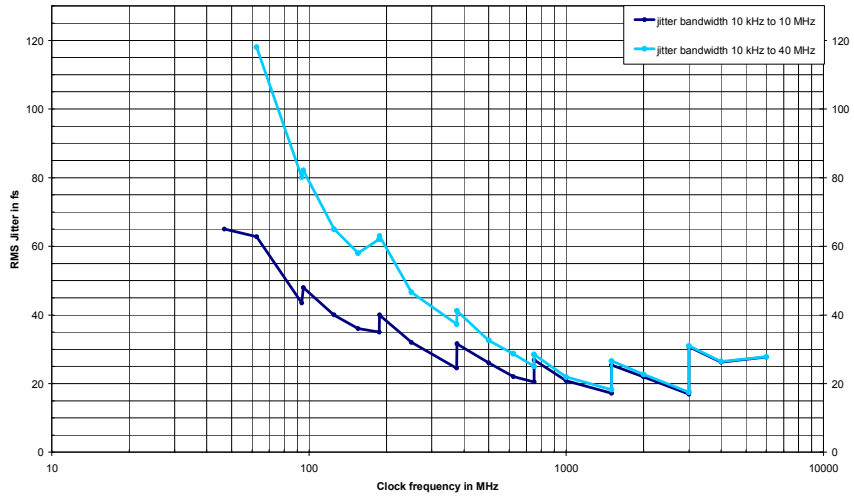

Fig. 34: RMS jitter vs. clock frequency for the R&S®SMA100A with R&S®SMA-B22 enhanced phase noise performance option.

6.1.5 SNR Due to Phase Noise for the R&S®SMA100A as Clock Source

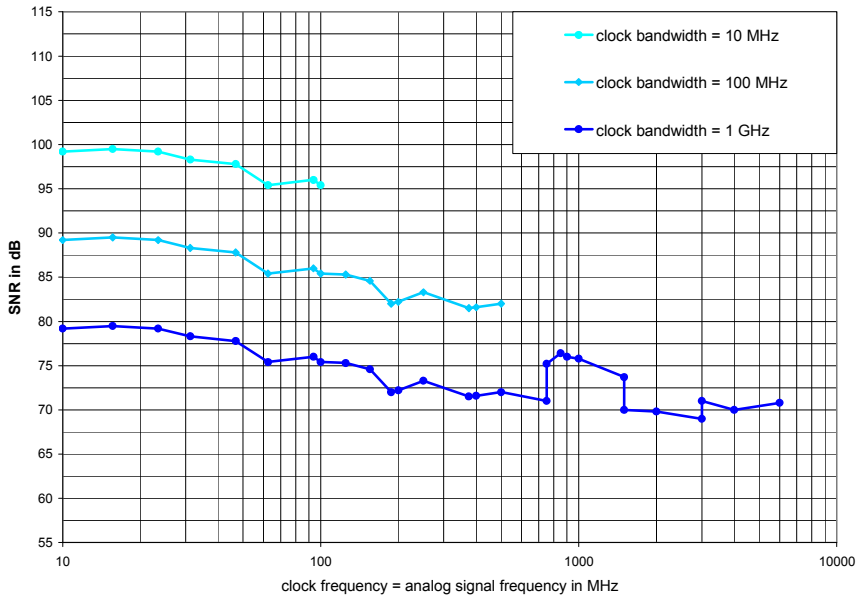

Fig. 35: SNR vs. clock rate and clock bandwidth for the R&S®SMA100A and fanalog = fclk.

6.1.6 SNR Due to Wideband Noise for the R&S®SMA100A as Analog Source

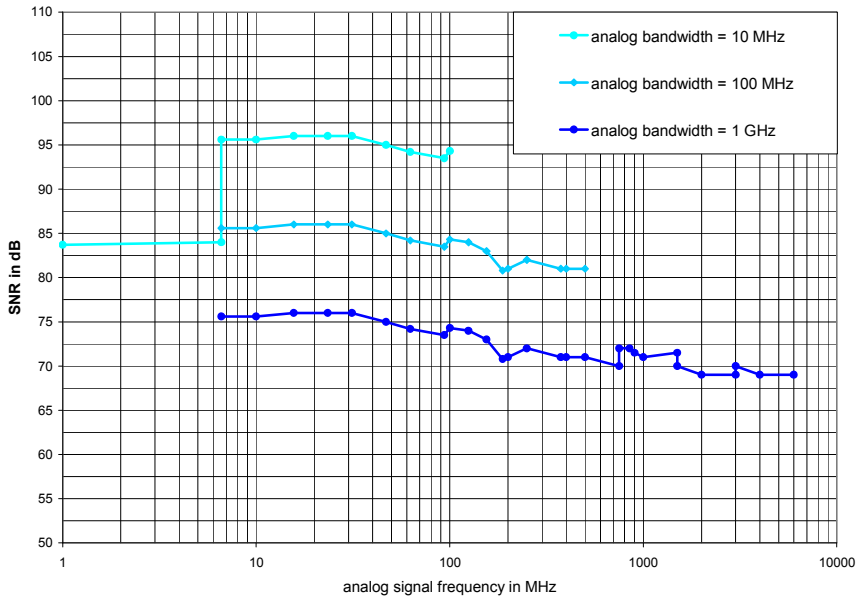

Fig. 36: SNR vs. analog signal frequency and analog bandwidth for the R&S®SMA100A.

6.1.7 SNR Due to Non-Harmonics

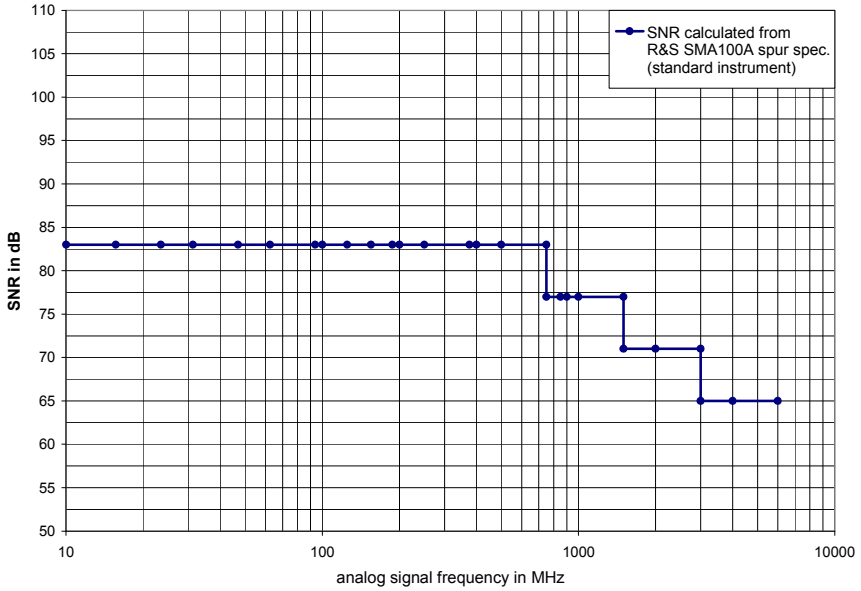

Fig. 37: SNR performance of the R&S®SMA100A due to a non-harmonic spurious vs. analog signal frequency (standard instrument).

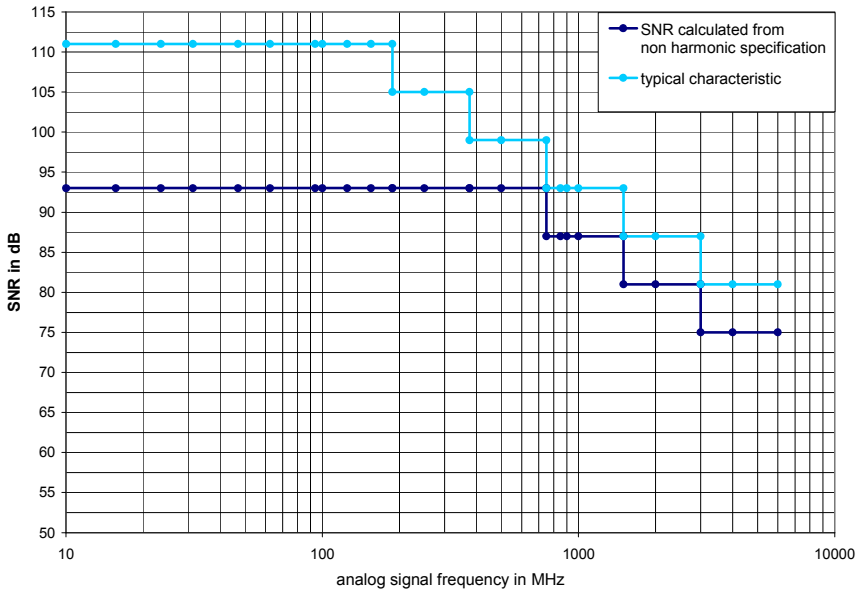

Fig. 38: SNR performance of the R&S®SMA100A due to a non-harmonic spurious vs. analog signal frequency with the R&S®SMA-B22 option for enhanced phase noise performance.

6.1.8 SFDR Due to Non-Harmonics

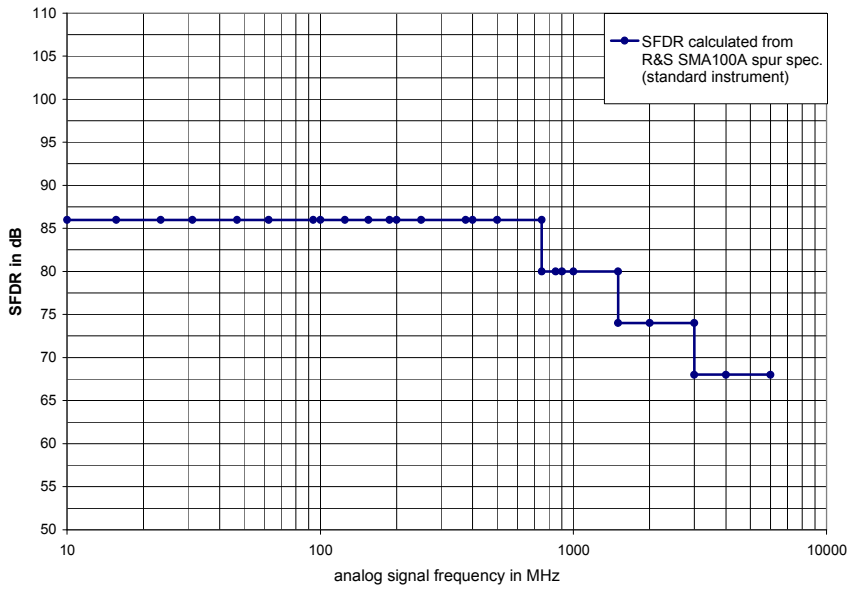

Fig. 39: SFDR performance of the R&S®SMA100A due to a non-harmonic spurious vs. analog signal frequency (standard instrument).

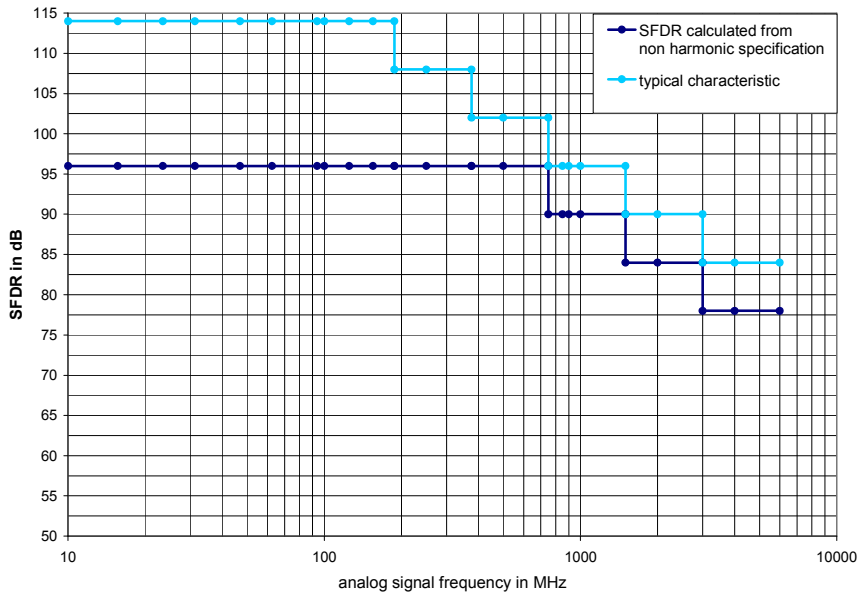

Fig. 40: SFDR performance of the R&S®SMA100A due to a non-harmonic spurious vs. analog signal frequency with R&S®SMA-B22 enhanced phase noise performance option.

6.1.9 Harmonics

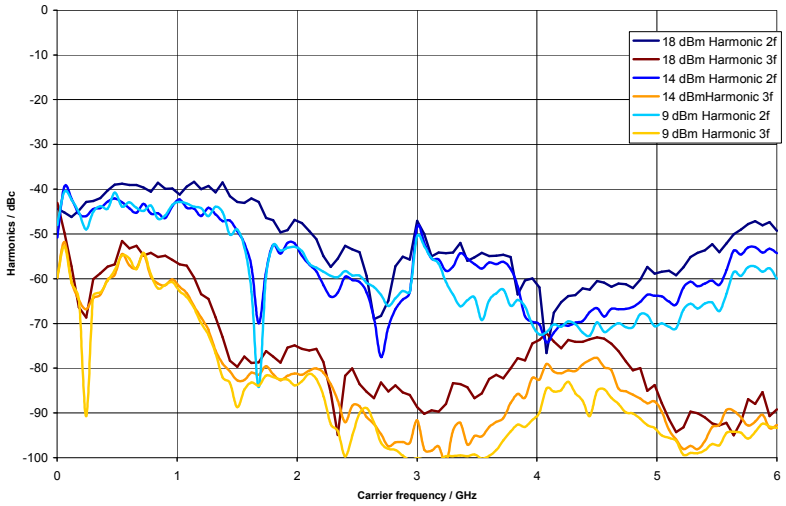

Fig. 41: Measured harmonics vs. carrier frequency and output level for the R&S®SMA100A.

6.2 Performance Data for Option R&S®SMA-B29 (Clock Synthesizer)

6.2.1 SSB Phase Noise

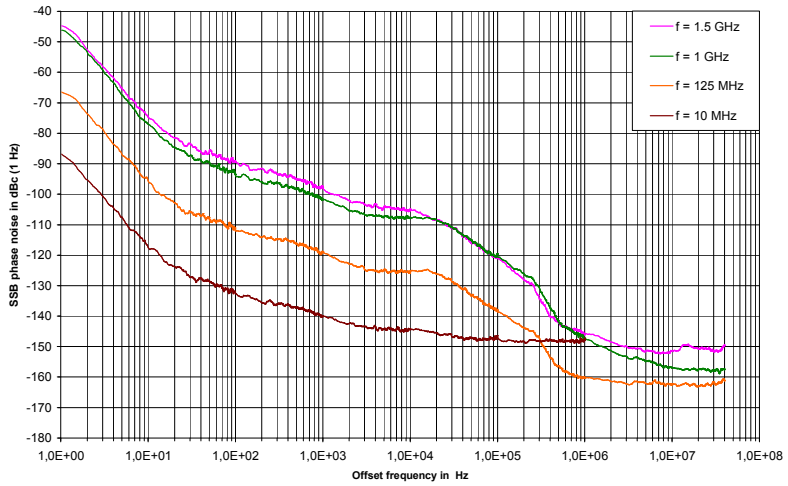

Fig. 42: R&S®SMA-B29 SSB phase noise (standard instrument).

6.2.2 Wideband SSB Phase Noise

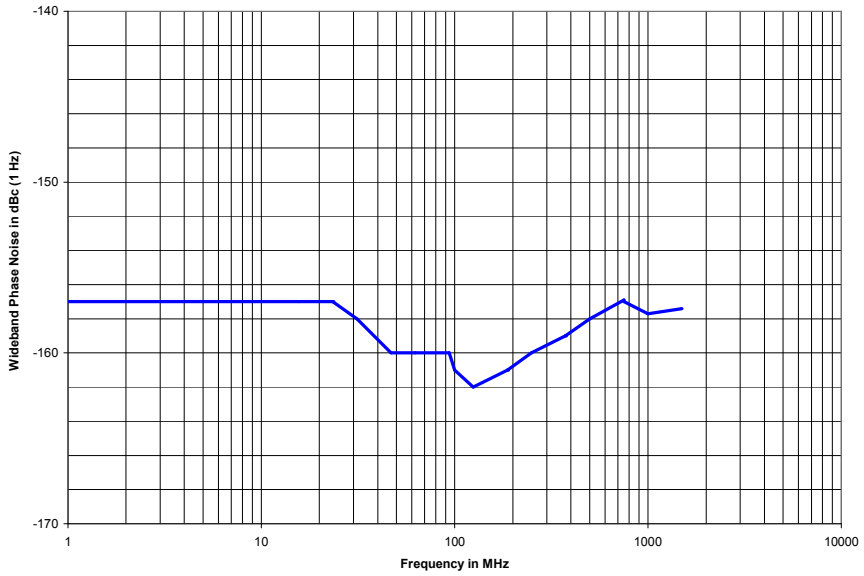

Fig. 43: R&S®SMA-B29 wideband phase noise performance option.

6.2.3 Wideband Noise

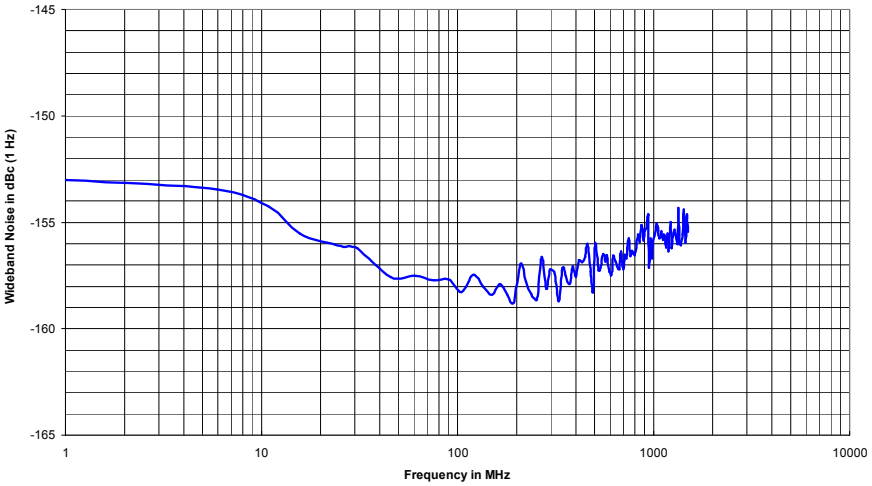

Fig. 44: R&S®SMA-B29: overall wideband noise vs. carrier frequency.

6.2.4 RMS Jitter (Bandwidth 10 kHz to 10 MHz and 10 kHz to 40 MHz)

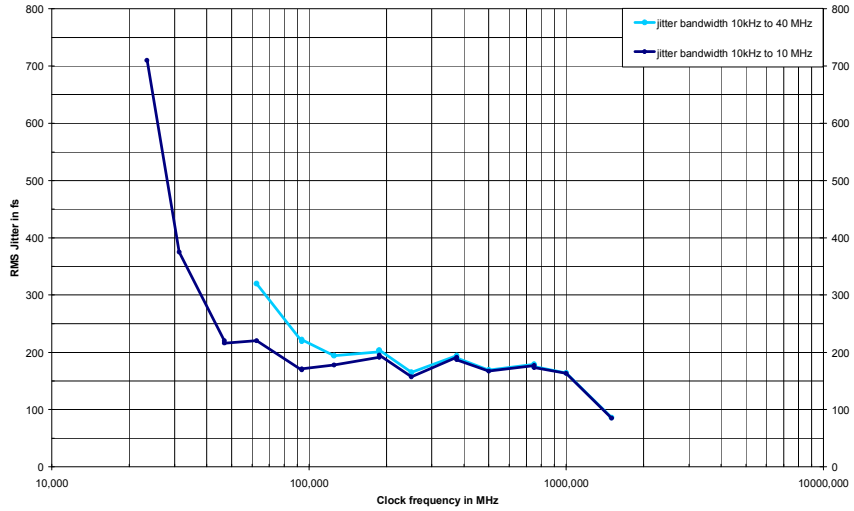

Fig. 45: RMS jitter vs. clock frequency for R&S®SMA-B29.

6.2.5 SNR Due to Phase Noise for R&S®SMA-B29 as Clock Source

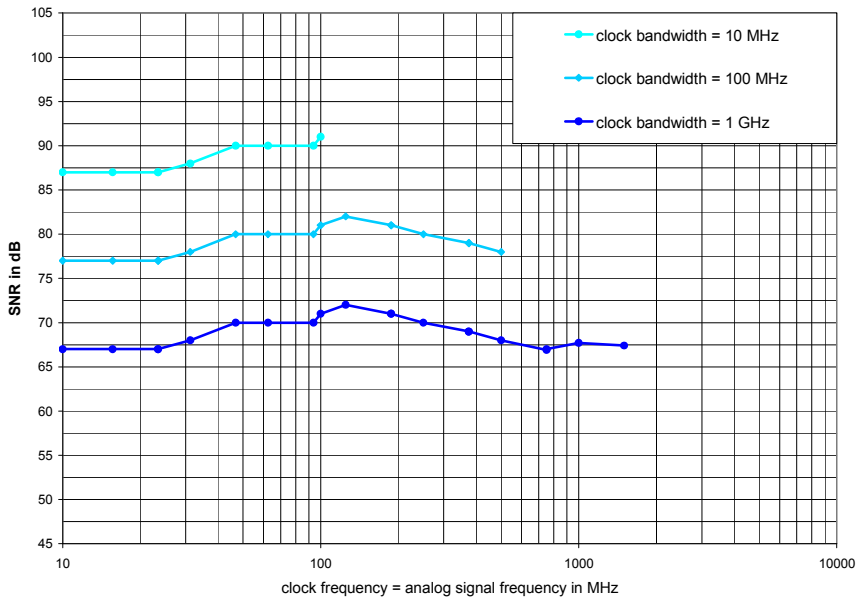

Fig. 46: SNR vs. clock rate and clock bandwidth for R&S®SMA-B29 and fanalog = fclk.

6.2.6 SNR Due to Non-Harmonics

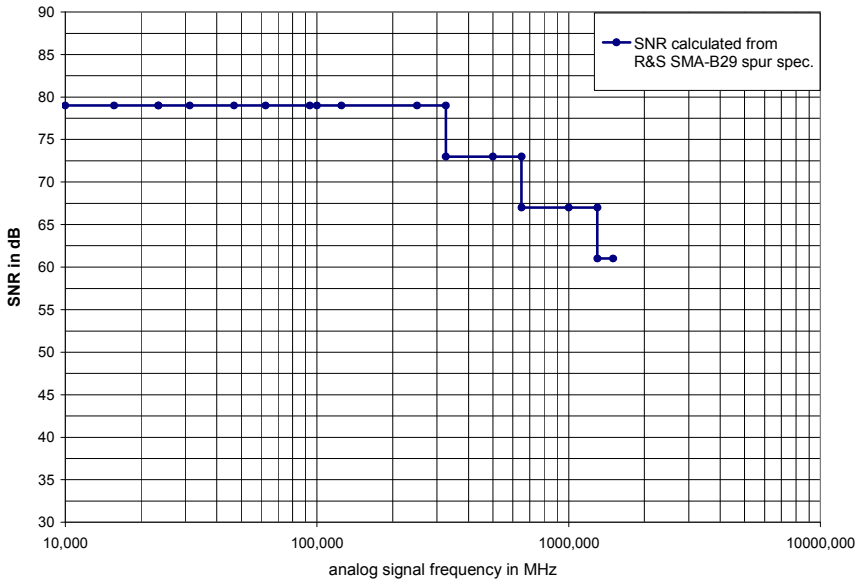

Fig. 47: SNR performance of R&S®SMA-B29 due to a non-harmonic spurious vs. analog signal frequency.

6.2.7 SFDR Due to Non-Harmonics

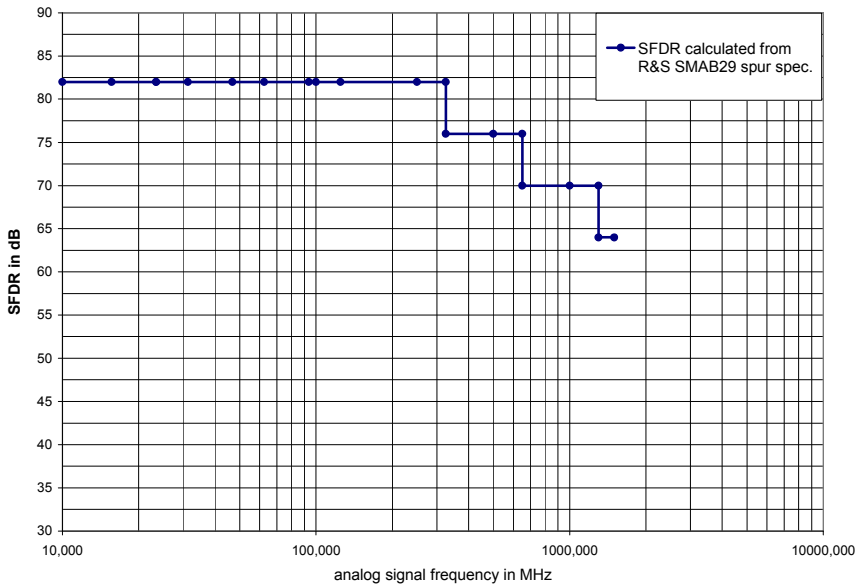

Fig. 48: SFDR performance of R&S®SMA-B29 due to a non-harmonic spurious vs. analog signal frequency.

6.2.8 Harmonics

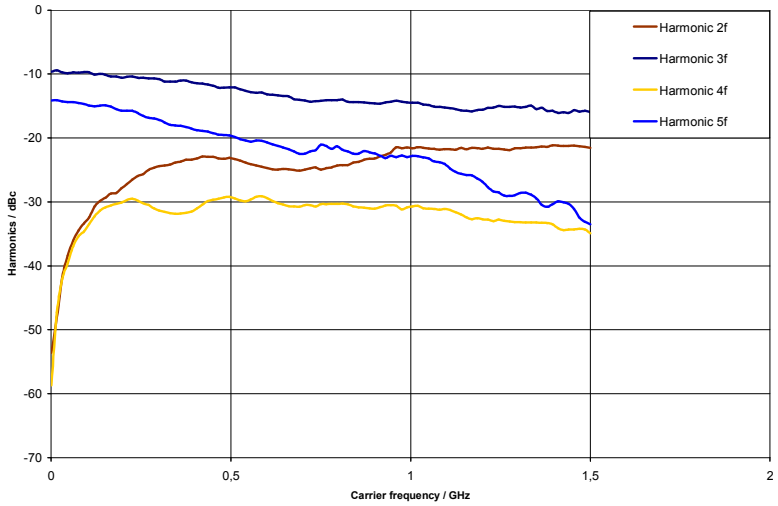

Fig. 49: Measured harmonics vs. carrier frequency for R&S®SMA-B29.

6.3 Performance Data for the R&S®SMB100A

6.3.1 SSB Phase Noise

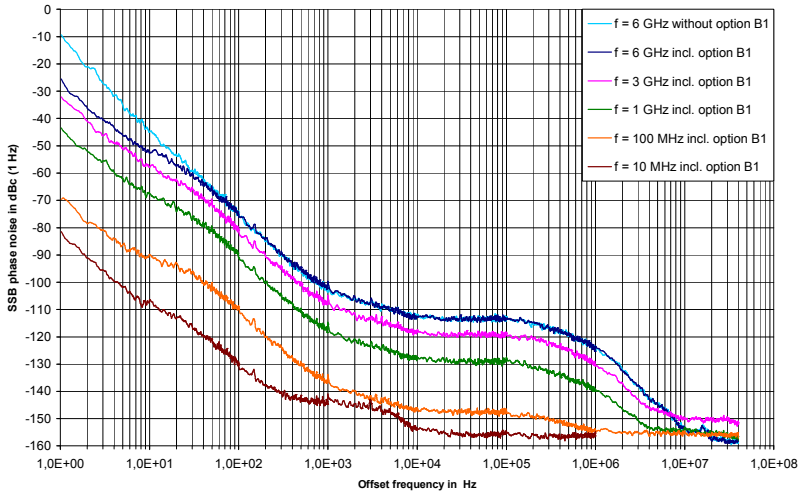

Fig. 50: R&S®SMB100A SSB phase noise with the R&S®SMB-B1 option (at 6 GHz also without the R&S®SMB-B1 option).

6.3.2 Wideband SSB Phase Noise

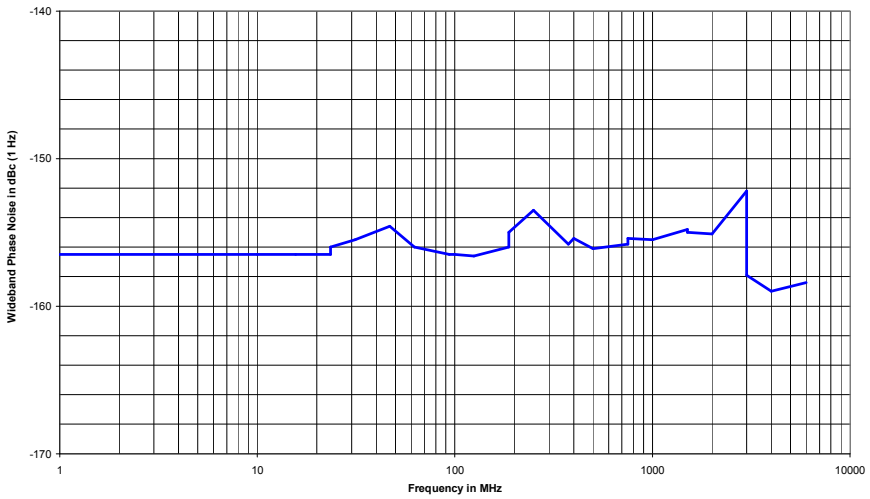

Fig. 51: R&S®SMB100A wideband phase noise performance.

6.3.3 Wideband Noise

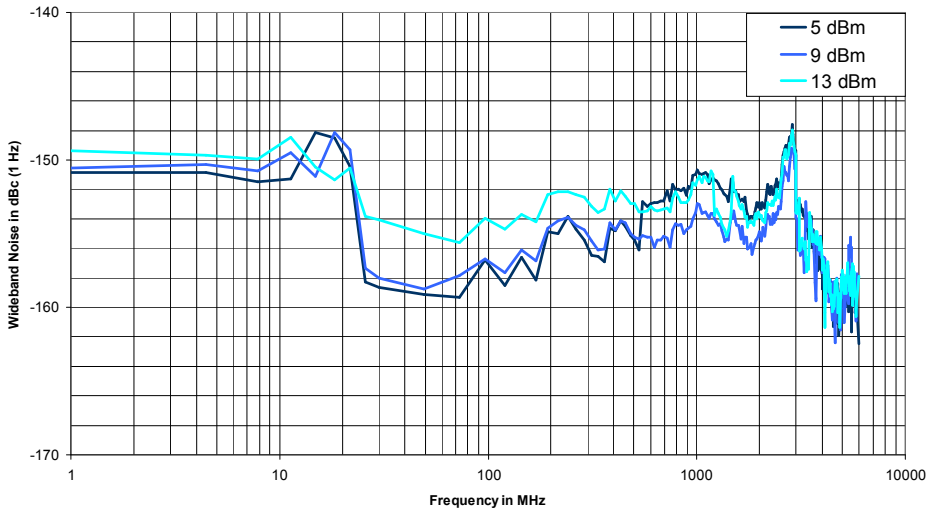

Fig. 52: R&S®SMB100A overall wideband noise vs. carrier frequency and output level.

6.3.4 RMS Jitter (Bandwidth 10 kHz to 10 MHz and 10 kHz to 40 MHz)

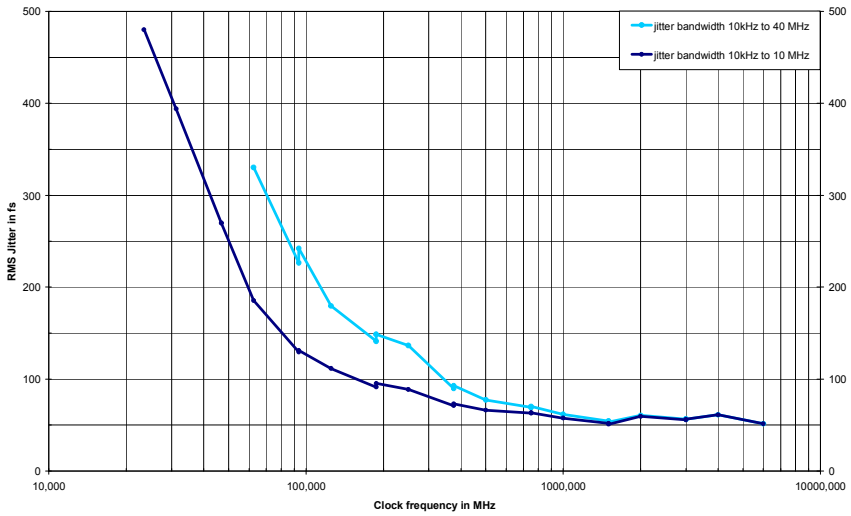

Fig. 53: RMS jitter vs. clock frequency for the R&S®SMB100A.

6.3.5 SNR Due to Phase Noise for the R&S®SMB100A as Clock Source

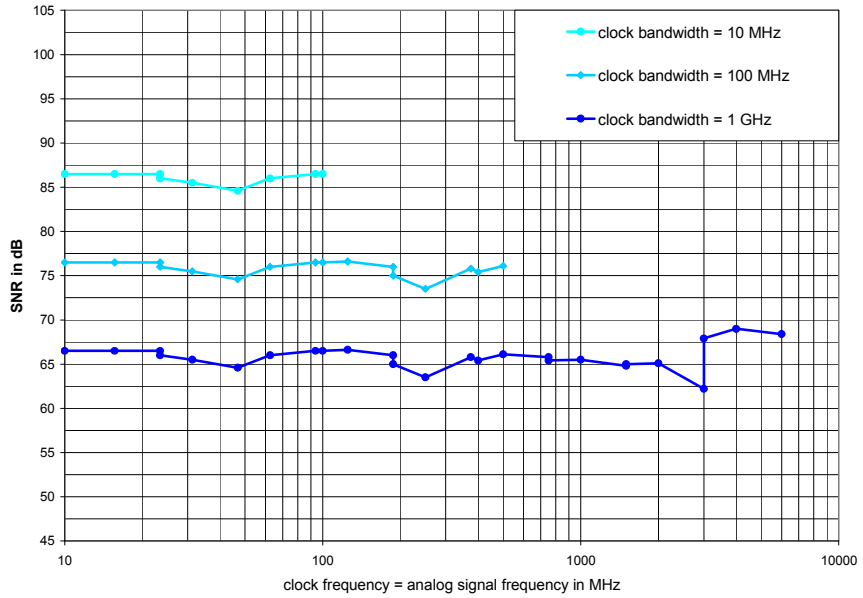

Fig. 54: SNR vs. clock rate and clock bandwidth for the R&S®SMB100A and fanalog = fclk.

6.3.6 SNR Due to Wideband Noise for the R&S®SMB100A as Analog Source

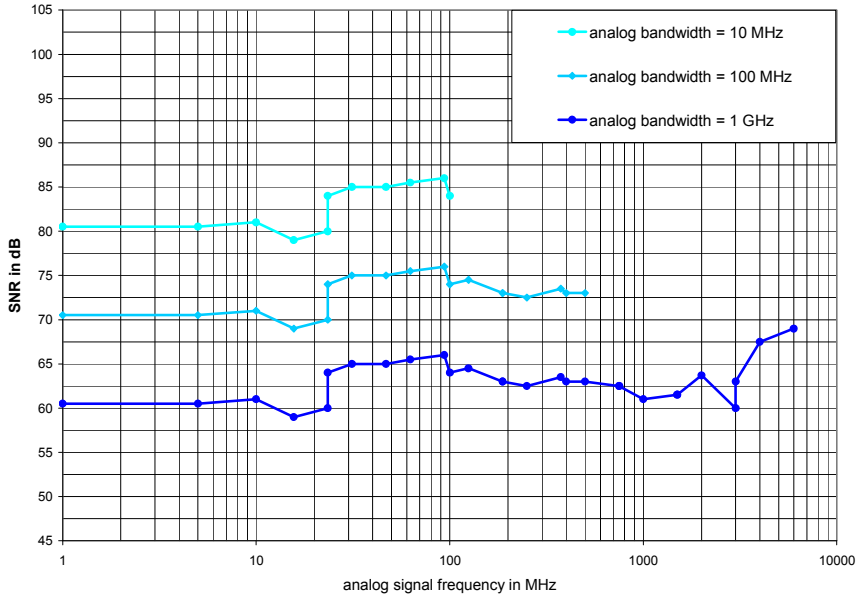

Fig. 55: SNR vs. analog signal frequency and analog bandwidth for the R&S®SMB100A.

6.3.7 SNR Due to Non-Harmonics

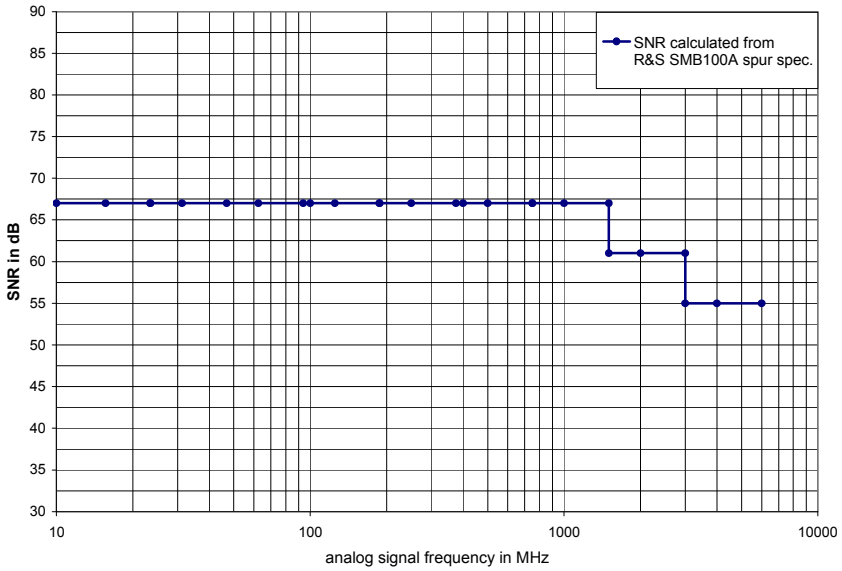

Fig. 56: SNR performance of the R&S®SMB100A due to a non-harmonic spurious vs. analog signal frequency.

6.3.8 SFDR Due to Non-Harmonics

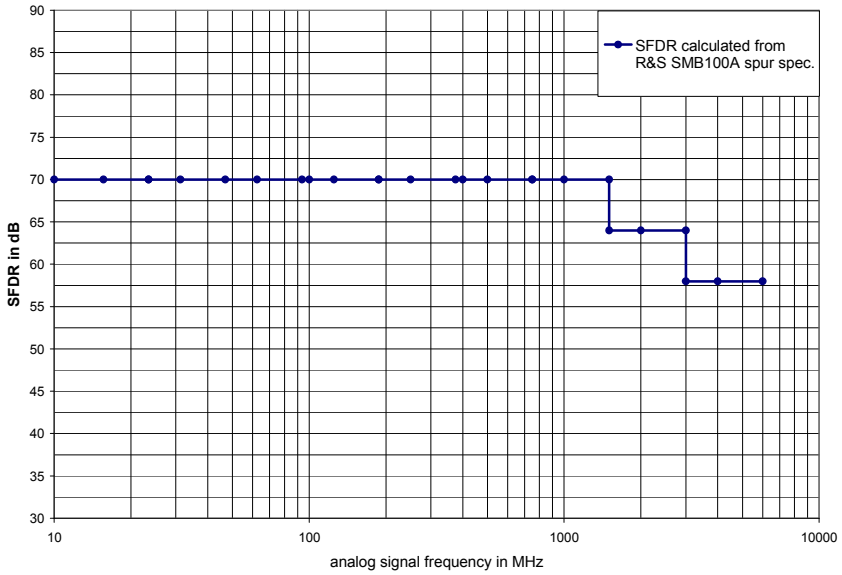

Fig. 57: SFDR performance of the R&S®SMB100A due to a non-harmonic spurious vs. analog signal frequency.

6.3.9 Harmonics

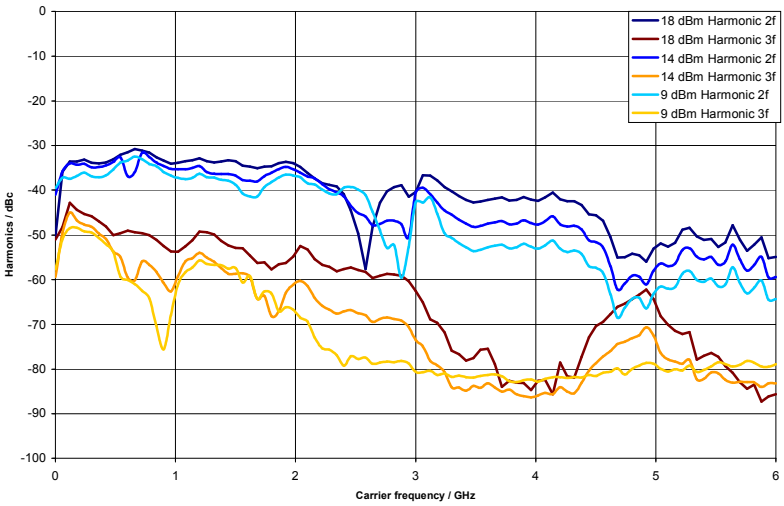

Fig. 58: Measured harmonics vs. carrier frequency and output level for the R&S®SMB100A.

6.4 Performance Data for the R&S®SMC100A

6.4.1 SSB Phase Noise

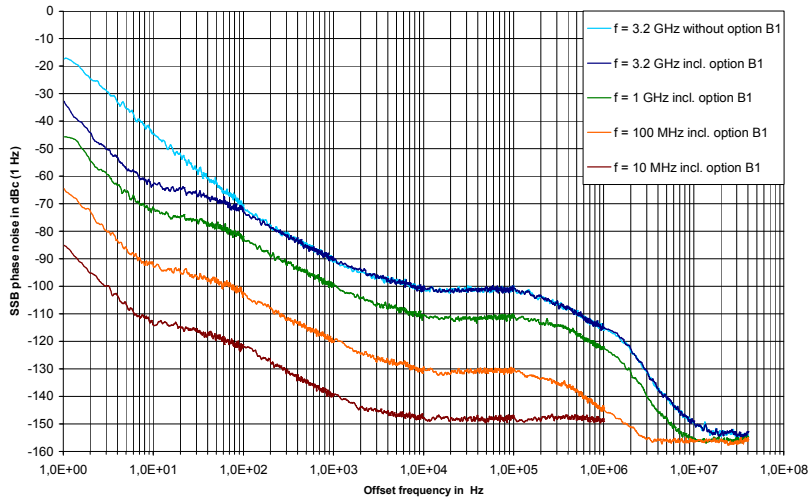

Fig. 59: R&S®SMC100A SSB phase noise with R&S®SMB-B1 option (at 6 GHz also without R&S®SMB-B1 option).

6.4.2 Wideband SSB Phase Noise

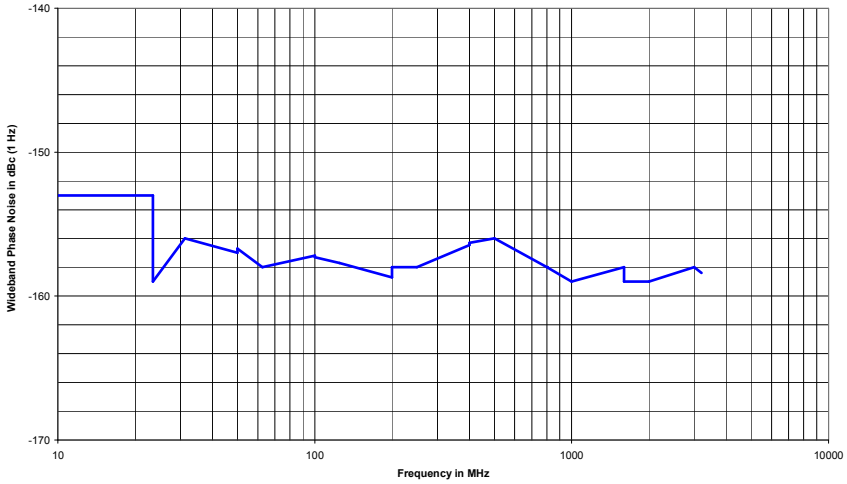

Fig. 60: R&S®SMC100A wideband phase noise performance.

6.4.3 Wideband Noise

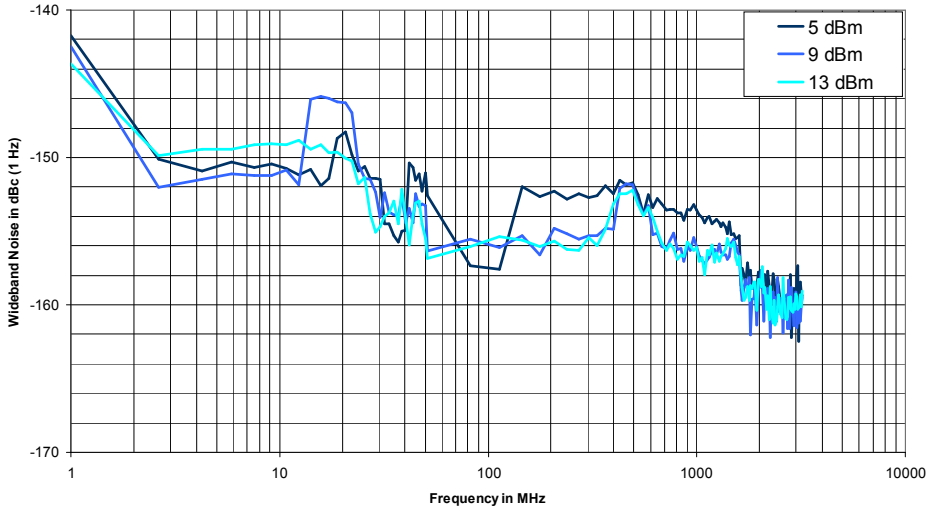

Fig. 61: R&S®SMC100A overall wideband noise vs. carrier frequency and output level.

6.4.4 RMS Jitter (Bandwidth 10 kHz to 10 MHz and 10 kHz to 40 MHz)

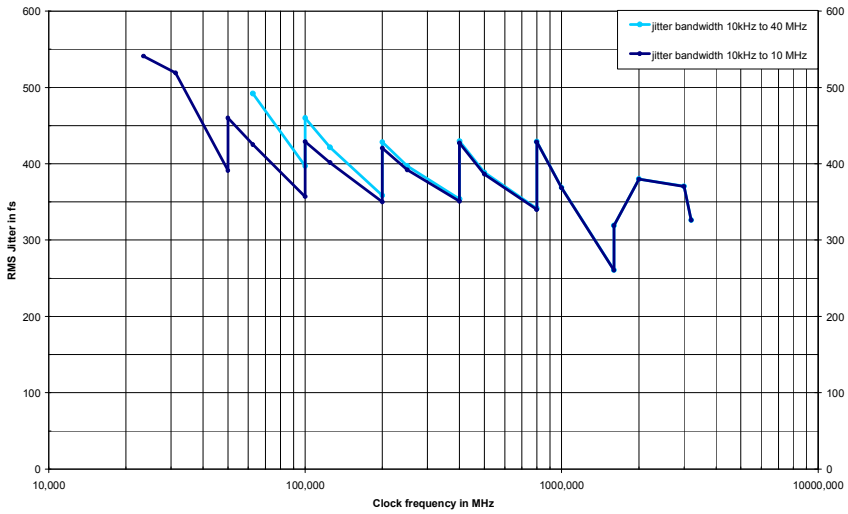

Fig. 62: RMS jitter vs. clock frequency for the R&S®SMC100A.

6.4.5 SNR Due to Phase Noise for the R&S®SMC100A as Clock Source

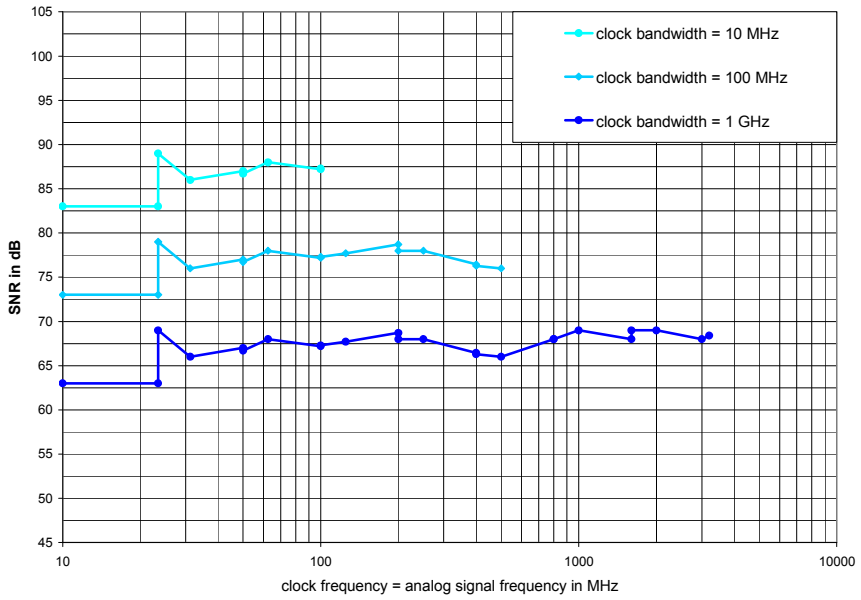

Fig. 63: SNR vs. clock rate and clock bandwidth for the R&S®SMC100A and fanalog = fclk.

6.4.6 SNR Due to Wideband Noise for the R&S®SMC100A as Analog Source

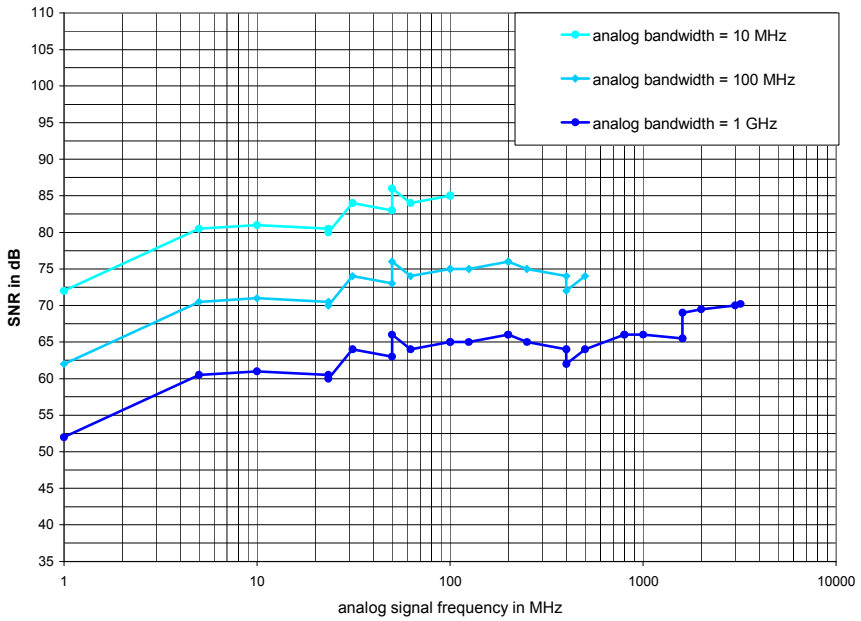

Fig. 64: SNR vs. analog signal frequency and analog bandwidth for the R&S®SMC100A.

6.4.7 SNR Due to Non-Harmonics

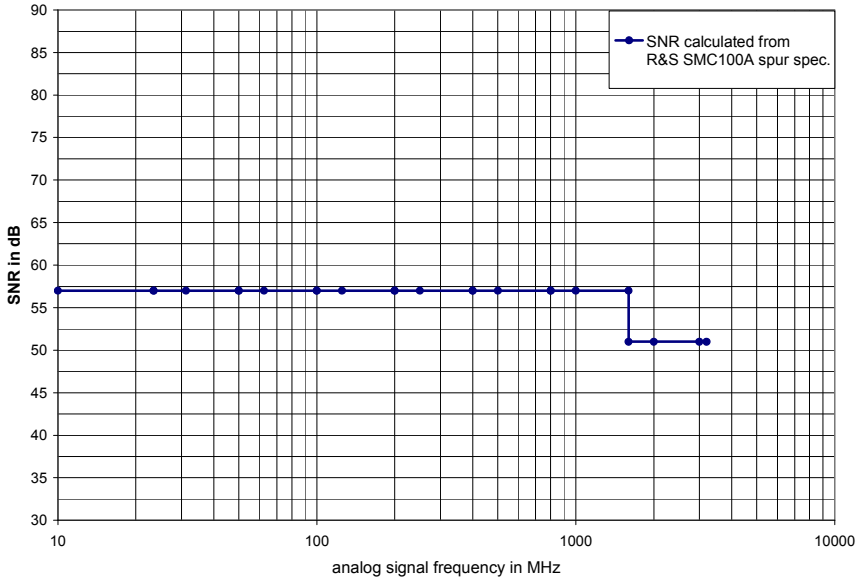

Fig. 65: SNR performance of the R&S®SMC100A due to a non-harmonic spurious vs. analog signal frequency.

6.4.8 SFDR Due to Non-Harmonics

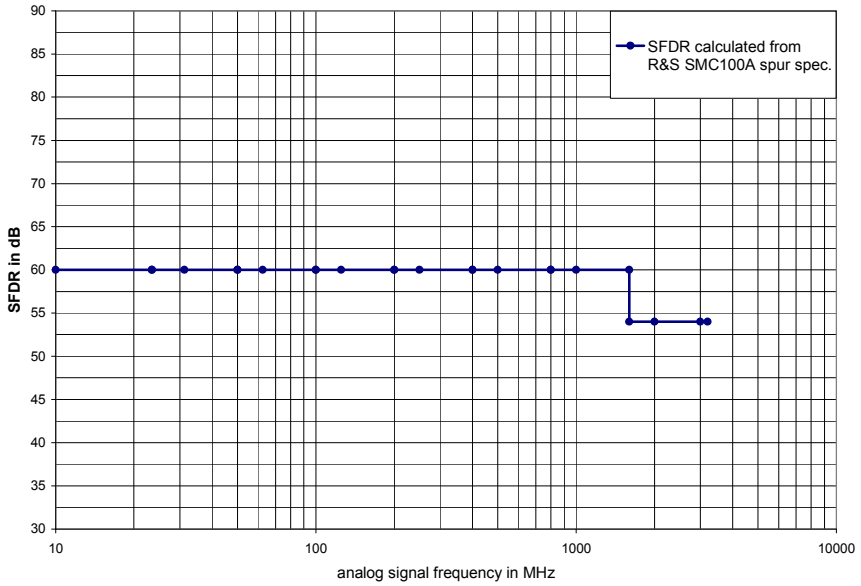

Fig. 66: SFDR performance of the R&S®SMC100A due to a non-harmonic spurious vs. analog signal frequency.

6.4.9 Harmonics

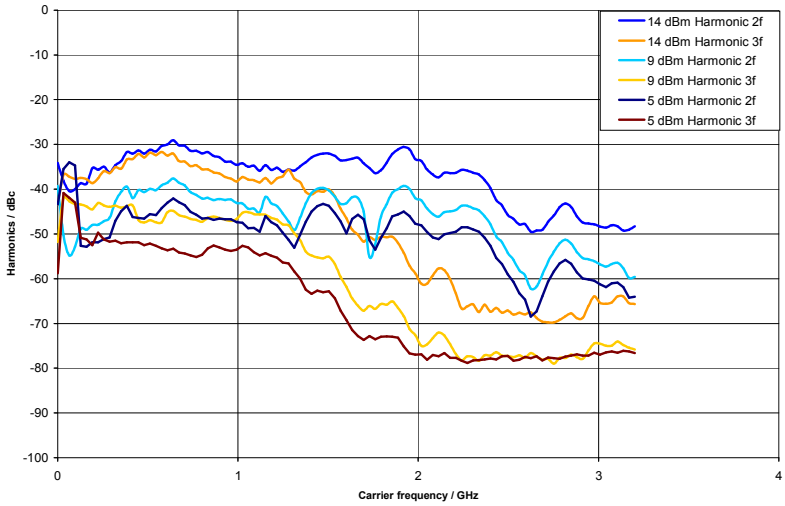

Fig. 67: Measured harmonics vs. carrier frequency and output level for the R&S®SMC100A.

7 Literature

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6. Data Sheet AD9445, 14-Bit, 125 MSPS ADC, Analog Devices, 2005

7. R&S®SMA100A Signal Generator Data Sheet
www.rohde-schwarz.com/product/SMA100A

8. R&S®SMB100A Signal Generator Data Sheet
www.rohde-schwarz.com/product/SMB100A

9. R&S®SMC100A Signal Generator Data Sheet
www.rohde-schwarz.com/product/SMC100A

8 Ordering Information

Type of Instrument

Instrument	Designation	Ordering No
R&S®SMA100A	Signal Generator base unit requires RF path	1400.0000.02
R&S®SMA-B103	RF path 9 kHz to 3 GHz, with electronic attenuator	1405.0209.02
R&S®SMA-B106	RF path 9 kHz to 6 GHz, with electronic attenuator	1405.0809.02
R&S®SMA-B22	Option: Enhanced Phase Noise Performance and FM/PHIM Modulator	1405.1805.02
R&S®SMA-B29	Option: Clock Synthesizer	1405.2503.02
R&S®SMB100A	Signal Generator base unit, requires RF path	1406.6000.02
R&S®SMB-B101	RF path 9 kHz to 1.1 GHz,	1407.2509.02
R&S®SMB-B102	RF path 9 kHz to 2.2 GHz,	1407.2609.02
R&S®SMB-B103	RF path 9 kHz to 3.2 GHz,	1407.2709.02
R&S®SMB-B106	RF path 9 kHz to 6 GHz,	1407.2909.02
R&S®SMC100A	Signal Generator base unit, requires RF path	1411.4002.02
R&S®SMC-B101	RF path 9 kHz to 1.1 GHz,	1411.6505.02
R&S®SMC-B103	RF path 9 kHz to 3.2 GHz,	1411.6605.02

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